

Quarterly Technical Report

Solid State Research

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Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LEXINGTON, MASSACHUSETTS



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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 AUGUST-31 OCTOBER 1996

ISSUED 9 JULY 1997

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LEXINGTON

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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 August through 31 October 1996. The topics covered are Quantum Electronics, Electrooptical Materials and Devices, Submicrometer Technology, High Speed Electronics, Microelectronics, Analog Device Technology, and Advanced Silicon Technology. Funding is provided primarily by the Air Force, with additional support provided by the Army, DARPA, Navy, BMDO, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

The frequency-doubled output of a high-power passively Q -switched Nd:YAG microlaser has been used to pump a KTP doubly resonant miniature monolithic Fabry-Perot (microchip) optical parametric oscillator with 20% conversion efficiency, generating the shortest pulses reported for an optical parametric oscillator pumped with individual Q -switched pulses. The 8.4- μ J, 600-ps pulses from the parametric oscillator were subsequently frequency quadrupled into the ultraviolet with 3% efficiency.

2. ELECTROOPTICAL MATERIALS AND DEVICES

Organometallic vapor phase epitaxy has been used to grow a $\text{Ga}_{0.87}\text{In}_{0.13}\text{As}_{0.12}\text{Sb}_{0.88}/\text{Al}_{0.06}\text{Ga}_{0.04}\text{As}_{0.05}\text{Sb}_{0.95}$ multiple-quantum-well diode laser structure. Devices emitting at 2.1 μm exhibit pulsed threshold current densities as low as 1.2 kA/cm^2 .

High-quality p -type $\text{Pb}_{1-x}\text{Eu}_x\text{Te}/\text{PbTe}$ multiple-quantum-well structures have been grown by molecular-beam epitaxy with two-dimensional thermoelectric power factors and figures of merit that are over 4 \times better than those of the best bulk PbTe. A room-temperature power factor $P_{\text{F2D}} = 160 \mu\text{Wcm}^{-1}\text{K}^{-2}$ was measured and a 400-K figure of merit $Z_{2\text{D}}T > 2.3$ was estimated for the p -type quantum wells.

3. SUBMICROMETER TECHNOLOGY

Plasma-enhanced chemical-vapor-deposition techniques have been developed to deposit thin film materials with low thermal conductivity for microbolometer applications. A new instrument, based on photoacoustic measurements, was used to characterize the thermal conductivity of these films.

4. HIGH SPEED ELECTRONICS

A new enhancement-mode GaAs pseudomorphic high-electron-mobility transistor (pHEMT) with a low-temperature-grown (LTG) GaAs gate insulator has been developed, in which the source and drain are doped by a self-aligned implant and no gate recess is needed. The LTG-GaAs gate insulator drastically reduces the gate leakage current, allowing a maximum drain current of 390 mA/mm obtained at 3 V of forward gate bias; the maximum transconductance is 330 mS/mm and the cutoff frequency is 14.3 GHz for pHEMTs with a 0.5- μm gate length.

5. MICROELECTRONICS

A high-frame-rate, high-sensitivity and low-noise digital camera system with multiple operating modes has been developed for use in a visible wavefront sensor. The camera system consists of a back-illuminated 128×128 -pixel charge-coupled device imager with an integrated shutter and an electronic board set with flexible digital timing and low-noise video post-processing circuitry.

6. ANALOG DEVICE TECHNOLOGY

A new self-aligned planar fabrication process for monolithic circuits based on resonant-tunneling diodes has been developed. Compared to previous techniques, this process provides significantly improved device uniformity.

7. ADVANCED SILICON TECHNOLOGY

A 1.3-GHz silicon-on-insulator (SOI) CMOS chip has been designed and tested to demonstrate the suitability of the SOI CMOS process for a compressive receiver system being developed based on a superconducting chirp filter. The chip contains circuits similar to those needed for processing the digital signals that will be produced by the front end of the compressive receiver.

REPORTS ON SOLID STATE RESEARCH

1 AUGUST THROUGH 31 OCTOBER 1996

PUBLICATIONS

- | | | |
|--|---|--|
| High CW Power (> 200 mW/Facet)
at 3.4 μm from InAsSb/InAlAsSb
Strained Quantum Well Diode
Lasers | H. K. Choi
G. W. Turner
M. J. Manfra | <i>Electron. Lett.</i> 32 , 1296
(1996) |
| Ferrite-Superconductor Devices for
Advanced Microwave Applications | G. F. Dionne
D. E. Oates
D. H. Temme
J. A. Weiss | <i>IEEE Trans. Microwave
Theory Tech.</i> 44 , 1361
(1996) |
| Nondegenerate Four-Wave Mixing
Wavelength Conversion in Low-Loss
Passive InGaAsP-InP Quantum-
Well Waveguides | J. P. Donnelly
H. Q. Le
E. A. Swanson
S. H. Groves
A. Darwish*
E. P. Ippen* | <i>IEEE Photon. Technol. Lett.</i>
8 , 623 (1996) |
| High-Power 1.3- μm InGaAsP-InP
Amplifiers with Tapered Gain
Regions | J. P. Donnelly
J. N. Walpole
G. E. Betts
S. H. Groves
J. D. Woodhouse
F. J. O'Donnell
L. J. Missaggia
R. J. Bailey
A. Napoleone | <i>IEEE Photon. Technol. Lett.</i>
8 , 1450 (1996) |
| Fabrication and Theory of Diamond
Emitters | M. W. Geis
J. C. Twichell
T. M. Lyszczarz | <i>Lincoln Laboratory J.</i>
8 , 161 (1995) |

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- | | | |
|---|--|---|
| Light Scattering in High-Dislocation-Density GaN | Z. L. Liao
R. L. Aggarwal
P. A. Maki
R. J. Molnar
J. N. Walpole
R. C. Williamson
I. Melngailis | <i>Appl. Phys. Lett.</i> 69 , 1665 (1996) |
| Optoelectronic and Structural Properties of High-Quality GaN Grown by Hydride Vapor Phase Epitaxy | R. J. Molnar
R. Aggarwal
Z. L. Liao
E. R. Brown
I. Melngailis
W. Götz*
L. T. Romano*
N. M. Johnson* | <i>Mater. Res. Soc. Symp. Proc.</i> 395 , 189 (1996) |
| Hydride Vapor Phase Epitaxy of Gallium Nitride Films for Quasi-Bulk Substrates | R. J. Molnar
W. Götz*
L. T. Romano*
N. M. Johnson* | <i>Electrochem. Soc. Proc.</i> 96-11 , 212 (1996) |
| An Optical Correlator Using a Low-Temperature-Grown GaAs Photoconductor | S. Verghese
N. Zamdmer*
Q. Hu*
E. R. Brown
A. Forster* | <i>Appl. Phys. Lett.</i> 69 , 842 (1996) |
| Diffraction-Limited 1.3- μ m-Wavelength Tapered-Gain-Region Lasers with > 1-W CW Output Power | J. N. Walpole
J. P. Donnelly
S. H. Groves
L. J. Missaggia
J. D. Woodhouse
R. J. Bailey
A. Napoleone | <i>IEEE Photon. Technol. Lett.</i> 8 , 1429 (1996) |
| Lattice-Matched GaSb/AlGaAsSb Double-Heterostructure Diode Lasers Grown by MOVPE | C. A. Wang
H. K. Choi | <i>Electron. Lett.</i> 32 , 1779 (1996) |
| Ultraviolet Generation with Passively Q-Switched Microchip Lasers | J. J. Zayhowski | <i>Opt. Lett.</i> 21 , 1618 (1996) |

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ACCEPTED FOR PUBLICATION

Use of CCD Imagers for Charged-Particle Spectroscopy	B. E. Burke R. D. Petrasso* C. K. Li* T. C. Hotaling	<i>Rev. Sci. Instrum.</i>
Mid Infrared Semiconductor Lasers	H. K. Choi	<i>Rev. Laser Eng.</i>
Superconductivity for Improved Microwave Ferrite Devices	G. F. Dionne D. H. Temme D. E. Oates J. A. Weiss	<i>Lincoln Laboratory J.</i>
Calorimetric Measurements of Optical Materials for 193 nm Lithography	A. Grenville R. Uttaro J. H. C. Sedlacek M. Rothschild D. Corliss	<i>J. Vac. Sci. Technol. B</i>
Identification and Modeling of Microwave Loss Mechanisms in $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$	J. Herd* D. E. Oates J. Halbritter*	<i>IEEE Trans. Appl. Supercond.</i>
Plasma-Deposited Silylation Resist for 193-nm Lithography	M. W. Horn B. E. Maxwell R. B. Goodman R. R. Kunz L. M. Eriksen	<i>J. Vac. Sci. Technol. B</i>
Status of 193-nm Lithography Development at Lincoln Laboratory	R. R. Kunz J. A. Burns S. G. Cann C. L. Keast M. W. Horn S. C. Palmateer M. Rothschild D. C. Shaver	<i>Jpn. J. Appl. Phys.</i>

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Broad Wavelength Tunability
of Grating-Coupled External Cavity
Mid-Infrared Semiconductor Lasers

H. Q. Le
G. W. Turner
J. R. Ochoa
M. J. Manfra
C. C. Cook
Y.-H. Zhang*

Appl. Phys. Lett.

Simple Compact Diode Laser-
Microlens Packaging

Z-L. Liao
D. Z. Tsang*
J. N. Walpole

IEEE J. Quantum Electron.

High- T_c Superconductive Wideband
Compressive Receivers

W. G. Lyons
D. R. Arsenault
A. C. Anderson
P. G. Murphy
R. W. Ralston
M. M. Seaver
R. L. Slattery
T. C. L. G. Sollner

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Wideband Compressive Receiver
Based on Advanced Superconductor
and Semiconductor Circuits

W. G. Lyons
D. R. Arsenault
T. C. L. G. Sollner
R. W. Ralston

*IEEE Trans. Appl.
Supercond.*

X-Ray Photo Emission Spectroscopy
Study of Oxidized GaN

R. J. Molnar

Appl. Phys. Lett.

Superconductivity for Improved
Microwave Ferrite Devices

D. E. Oates
G. F. Dionne
D. H. Temme
J. A. Weiss

Lincoln Laboratory J.

Power Dependence of Microwave
 Z_s in High- T_c Josephson Junctions:
Measurements and Modeling

D. E. Oates
Y. M. Habib*
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*IEEE Trans. Appl.
Supercond.*

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Sub-Poisson Statistics Observed
in an Electronically Shuttered and
Back-Illuminated CCD Pixel

R. K. Reich

IEEE Trans. Electron Devices

High Performance CCD Imager
Technology for Plasma Diagnostics

R. K. Reich
W. M. McGonagle
J. A. Gregory
R. W. Mountain
B. B. Kosicki
E. D. Savoye

Rev. Sci. Instrum.

How Practical Is 193-nm Lithography?

M. Rothschild
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PRESENTATIONS†

Calorimetric Measurements of Optical
Materials for 193 nm Lithography

A. Grenville
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All-Dry Resist Process for 193-nm
Lithography

M. W. Horn
R. R. Kunz
S. C. Palmateer
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Practical Implementation of a Top
Surface Imaging Silylation Resist
into Device Fabrication at 193 nm

S. C. Palmateer
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Laser Induced Damage in Optical
Materials

M. Rothschild
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2nd International Symposium
on 193 nm Lithography,
Colorado Springs, Colorado,
30 July–2 August 1996

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†Titles of presentations are listed for information only. No copies are available for distribution.

Thin Film Superconducting Filters
for PCS Transmit Applications

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Development of Superconductive
Circuit Components for Sensing
and Routing Data in a Switching
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RF Power Dependence Study of
Large Area YBCO Thin Films

Z. Ma*
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Superconductor Ferrite Phase Shifters
and Circulators

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Tunable YBCO Resonators on YIG
Substrates

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Mixed Analog Digital Niobium
Superconductive Circuits for a
2-Gigachip-per-Second Spread
Spectrum Modem

J. P. Sage
D. A. Feld

Applied Superconductivity
Conference,
Pittsburgh, Pennsylvania,
25-30 August 1996

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Microwave Ferrites for Cryogenic Applications	G. F. Dionne	International Conference on Ferrites, Bordeaux, France, 3-6 September 1996
Laser Induced Pellicle Damage at 193 nm	A. Grenville M. Rothschild J. H. C. Sedlacek D. Corliss P. Gardner*	Photomask Technology '96 Symposium, Redwood City, California, 18-20 September 1996
Optical Lithography in Semiconductor Manufacturing	M. Rothschild	Meeting of New England Chapter of Optical Society of America, Waltham, Massachusetts, 19 September 1996
Electron Emission from Diamond	M. W. Geis J. C. Twichell T. M. Lyszczarz	American Vacuum Society Meeting, Burlington, Massachusetts, 2 October 1996
Large-Area Back-Illuminated CCD	J. A. Gregory B. E. Burke R. W. Mountain B. B. Kosicki E. D. Savoye V. S. Dolat T. L. Lind A. H. Loomis D. J. Young G. A. Luppino* J. Tonry*	European Southern Observatory Workshop on Optical Detectors for Astronomy, Garching, Germany, 8-10 October 1996
Image Stabilization with the Orthogonal-Transfer CCD	J. Tonry* B. E. Burke	

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Photolithography at 193 nm—How
Mature Is It?

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Optical Society of America
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Science XII, Optics and
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Rochester, New York,
20-25 October 1996

193-nm Lithography

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ANALOG DEVICE TECHNOLOGY

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1. QUANTUM ELECTRONICS

1.1 MICROCHIP OPTICAL PARAMETRIC OSCILLATORS

Diode-pumped passively Q -switched Nd:YAG microlasers are compact, economical, all-solid-state sources of coherent, subnanosecond, multikilowatt pulses at high repetition rates [1],[2]. The high intensities generated by these devices at 1.064 μm has led to efficient harmonic generation [2],[3] and, recently, conversion into the mid infrared using single-pass parametric amplifiers [4],[5]. Here, we report the use of the frequency-doubled output of a high-power passively Q -switched Nd:YAG microlaser to pump a KTP doubly resonant miniature monolithic Fabry-Perot (microchip) optical parametric oscillator, and the subsequent frequency conversion of its output into the ultraviolet. These experiments generate the shortest pulses reported for an optical parametric oscillator pumped with Q -switched pulses, and demonstrate that it is possible to access any wavelength in the ultraviolet, visible, and near infrared with extremely compact optical systems.

In the limit of no pump depletion, no losses, and noncritical phase matching between the pump, signal, and idler wavelengths, and neglecting beam divergence, the intensity of a signal passing through a parametric gain medium is given by

$$I_s(z) = I_s(0) \cosh^2(\sqrt{KI_p}z) \quad , \quad (1.1)$$

where we have assumed no input at the idler wavelength and

$$K = \frac{8\pi^2 d_{\text{eff}}^2}{\epsilon_0 c \lambda_s \lambda_i n_s n_i n_p} \quad . \quad (1.2)$$

In these equations, d_{eff} is the effective nonlinear coefficient, ϵ_0 is the dielectric constant of free space, c is the speed of light, λ is the vacuum wavelength, n is the refractive index, and the subscripts s , i , and p refer to the signal, idler, and pump frequencies, respectively. For $\sqrt{KI_p}z > 1$,

$$I_s(z) \approx \frac{I_s(0)}{4} \exp(2\sqrt{KI_p}z) \quad . \quad (1.3)$$

If there is initially one photon at the signal wavelength, and threshold is defined as the pump intensity that results in a signal pulse energy $E_{s,p}$ the threshold pump intensity $I_{p,t}$ for a single-pass parametric amplifier is given by

$$I_{p,t} = \frac{1}{K} \left\{ \frac{1}{2l} \left[\ln \left(\frac{E_{s,t} \lambda_s}{hc} \right) + \ln(4) \right] \right\}^2 \quad , \quad (1.4)$$

where h is Planck's constant and l is the length of the gain medium. For a singly resonant Fabry-Perot optical parametric oscillator, the optical intensity generated during one pass seeds the next pass and, for a monolithic device,

$$I_{p,t} = \frac{1}{K} \left\{ \frac{n_p}{\tau_p c} \ln \left(\frac{E_{s,t} \lambda_s}{hc} \right) + \frac{1}{2l} [\ln(4) - \ln(R_s)] \right\}^2, \quad (1.5)$$

where τ_p is the duration of the pump pulse, R_s is the product of the reflectivities of the two mirrors at the signal wavelength, and single-pass pumping of the oscillator has been assumed. (In deriving this equation, the temporal profile of the pump pulse was modeled as a top hat.) For a doubly resonant oscillator, the threshold condition becomes

$$I_{p,t} = \frac{1}{K} \left\{ \frac{n_p}{\tau_p c} \left[\ln \left(\frac{E_{s,t} \lambda_s}{hc} \right) + \ln(4) \right] - \frac{1}{2l} \ln(R_{s,i}) \right\}^2, \quad (1.6)$$

where we have made the simplifying assumption that the reflectivities of the mirrors ($R_{s,i}$) are the same for the signal and idler wavelengths.

Equation (1.4) indicates that, under the conditions stated, the threshold for parametric amplification can be made arbitrarily low by increasing the length of the gain medium. However, in real applications, the useful length of the nonlinear crystal is limited by walkoff or beam divergence. Even when this is not the case, the cost of long nonlinear crystals can be considerable. One technique to increase the effective length of the nonlinear crystal is the multipass amplifier [5]. The other approach is the use of parametric oscillators.

For parametric oscillators, pump light must be present during the buildup time of the pulse, placing requirements on the pulse duration. As a result, the pump energy required to reach threshold goes through a minimum as the pulse width is changed, as can be seen from Equations (2.5) and (2.6). This is in contrast to harmonic generation or parametric amplification. Therefore, optimization of pump sources for parametric oscillators is different than for other nonlinear devices. Having said that, our initial demonstration of a microlaser-pumped optical parametric oscillator used a pump source designed for efficient harmonic generation, and not the present application. It had a pulse duration less than that which would result in the minimum threshold.

To take advantage of available crystals, the optical parametric oscillator was designed as a degenerate (or near degenerate) device to be pumped by the second harmonic of the microlaser output. It consisted of a 5-mm-long piece of KTP oriented for type II phase matching. The two faces of the crystal normal to the beam propagation were polished flat and parallel. The pump-side face was coated to be highly reflecting at the 1.064- μm oscillating wavelength while transmitting 75% of the 532-nm pump light. The output face was 50% reflecting at the oscillating frequency and antireflection coated for the pump.

The high-power passively Q -switched microlaser used to pump the parametric oscillator has been reported previously [4]. It consists of a 3-mm-thick piece of Nd:YAG, a 3-mm-thick piece of Cr⁴⁺:YAG, and a 6-mm-thick piece of Nd:YAG, bonded together in that order, with a 40% output coupler. Pumped with a fiber-coupled 12-W diode laser array, it produces 157- μJ , single-frequency, TEM₀₀ pulses at 1.064 μm . This output is frequency doubled, resulting in 86- μJ pulses of 800-ps duration at 532 nm. It is then spectrally filtered to remove the remaining 1.064- μm radiation and focused to reproduce the 80- μm radius of the 532-nm light exiting the frequency-doubling crystal, as shown in the left half of Figure 1-1. The

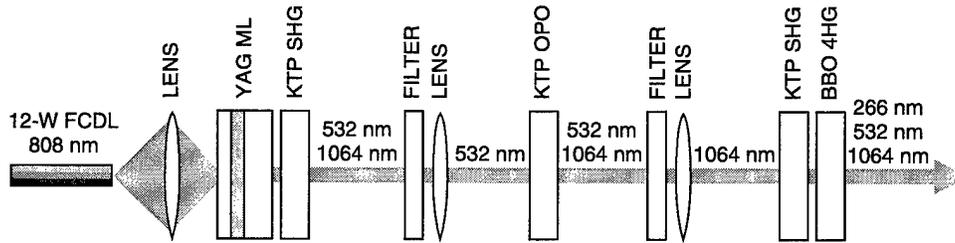


Figure 1-1. Experimental setup for frequency-quadrupled optical parametric oscillator pumped by second harmonic of a high-power diode-pumped passively *Q*-switched microlaser. FCDL, fiber-coupled diode laser; ML, microlaser; SHG, second-harmonic generator; OPO, optical parametric oscillator; 4HG, fourth-harmonic generator.

532-nm energy incident on the parametric oscillator was $56 \mu\text{J}/\text{pulse}$; the energy transmitted by the input coating was $42 \mu\text{J}/\text{pulse}$. At this pump level the oscillator was ~ 2.2 times above threshold and operated with 20% conversion efficiency. It generated $8.4 \mu\text{J}$ of $1.064\text{-}\mu\text{m}$ radiation, divided equally between the two orthogonal polarizations. The duration of the $1.064\text{-}\mu\text{m}$ pulses was 600 ps, and the output beam was better than 2 times diffraction limited.

Spectrally, the parametric oscillator operated in one of two modes. At times, it operated as a truly degenerate oscillator with both the signal and idler wavelength at $1.064 \mu\text{m}$, perhaps seeded by residual $1.064\text{-}\mu\text{m}$ radiation from the microlaser. In this mode the output was transform limited, and the pulse-to-pulse stability was excellent, with shot-to-shot energy variations of $< 1\%$. Once in this mode, the parametric oscillator typically remained there for tens of minutes to hours.

At other times the parametric oscillator operated in a nearly degenerate mode, with the signal and idler wavelengths separated by as much as 500 GHz. In this mode the signal and idler wavelengths would hop between approximately six adjacent cavity modes on a pulse-to-pulse basis (observed with a charge-coupled device (CCD) array and a $1/2\text{-m}$ grating spectrometer), with energy variations of $\sim 10\%$. Each pulse, however, was transform limited (measured using a CCD array and a high-*Q*, 1-cm solid etalon). The mode hopping is attributed to the use of a doubly resonant cavity with no thermal or acoustic isolation. It remains to be seen whether or not it can be eliminated. Singly resonant devices should have improved stability, at the expense of a higher threshold (see Figure 1-2).

The output of the parametric oscillator was frequency quadrupled into the ultraviolet with 3% efficiency. The $1.064\text{-}\mu\text{m}$ light was first filtered to remove the 532-nm pump light and focused to reproduce the waist dimensions of the light exiting the parametric oscillator. Properly oriented 5-mm-long, antireflection-coated crystals of KTP and BBO were positioned at the waist to perform the harmonic conversion [3]. The entire optical system is illustrated in Figure 1-1.

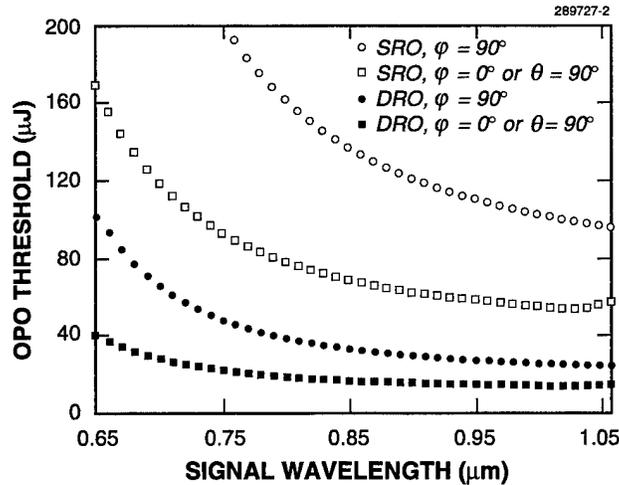


Figure 1-2. Calculated threshold for a doubly resonant (DRO) and singly resonant (SRO) KTP optical parametric oscillator pumped by a frequency-doubled microlaser. The 532-nm output of the pump source was assumed to have a 100- μm radius and 1-ns duration. Ten percent output coupling was used for the signal and idler wavelengths. The length of the KTP was set equal to the aperture length determined by walkoff, up to a maximum length of 1 cm. Threshold was set at 1 μJ of signal.

In all of the experiments with the parametric oscillator, care was taken to never focus the light more tightly than the light exiting the microlaser. All of the nonlinear crystal used could have been butt coupled to the laser, within the collimated region ($1/2$ the confocal parameter) of the laser output. Intervening optics were only used for experimental convenience. The optical head of a frequency-quadrupled optical parametric oscillator pumped by the second harmonic of a high-power diode-pumped passively Q -switched microlaser could be less than 3 in. long! And, all of the crystals used have flat faces, allowing for the economical fabrication associated with microchip devices.

Optical parametric devices afford microlaser systems enormous wavelength flexibility. Calculations, based on the Sellmeier coefficients reported by Vanherzeele et al. [6] for hydrothermally grown KTP and on the more conservative values $d_{15} = 2.6$ pm/V and $d_{24} = 3.3$ pm/V reported by Eckardt et al. [7], indicate that the frequency-doubled output of the high-power microlaser discussed above should be able to pump KTP parametric oscillators operating at wavelengths (both signal and idler) between 650 and 3000 nm (see Figure 1-2). The output of these devices can be harmonically converted into the visible and ultraviolet. Periodically poled lithium niobate parametric amplifiers, pumped by the 1.064- μm output of a microlaser, have already demonstrated the ability to operate at wavelengths between 1400 and 4400 nm [4].

One intriguing possibility is a microlaser system that generates red, green, and blue pulses. A KTP parametric oscillator pumped by the green output of a frequency-doubled microlaser can produce both

1.51- and 0.82- μm light. When summed with the 1.064- μm fundamental output of the microlaser (in KTP), these two wavelengths generate red and blue. Combined with the unused green pump light, this provides a compact three-color system.

The high performance, compact size, and potential low cost of microchip optical parametric oscillators, coupled with the reliability and efficiency of an all-solid-state system, make them attractive for industrial and field use. Potential applications include time-resolved excitation, absorption, and fluorescence spectroscopy; multicolor three-dimensional imaging; and displays.

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REFERENCES

1. J. J. Zayhowski and C. Dill III, *Opt. Lett.* **19**, 1427 (1994).
2. J. J. Zayhowski, *Laser Focus World*, 73, April 1996.
3. J. J. Zayhowski, *Opt. Lett.* **21**, 588 (1996); **21**, 1618 (1996).
4. J. J. Zayhowski, *Opt. Lett.* **22**, 169 (1997).
5. T. H. Jeys, *Opt. Lett.* **21**, 1229 (1996).
6. H. Vanherzeele, J. D. Bierlein, and F. C. Zumsteg, *Appl. Opt.* **27**, 3314 (1988).
7. R. C. Eckardt, H. Masuda, Y. X. Fan, and R. L. Byer, *IEEE J. Quantum Electron.* **26**, 922 (1990).

2. ELECTROOPTICAL MATERIALS AND DEVICES

2.1 GaInAsSb/AlGaAsSb MULTIPLE-QUANTUM-WELL DIODE LASERS GROWN BY ORGANOMETALLIC VAPOR PHASE EPITAXY

Previously, we reported the first lattice-matched GaSb/Al_{0.3}Ga_{0.7}As_{0.02}Sb_{0.98} double-heterostructure diode lasers grown by organometallic vapor phase epitaxy (OMVPE) [1]. These lasers operated at a wavelength of 1.75 μm with a threshold current density of 2.1 kA/cm². Here, we report the first GaInAsSb/AlGaAsSb multiple-quantum-well (MQW) diode lasers grown by OMVPE.

GaInAsSb and AlGaAsSb epitaxial layers were grown on (100) GaSb substrates, oriented 2° toward (110), in a vertical rotating-disk reactor operating at 150 Torr with H₂ as the carrier gas. GaInAsSb layers were grown with the novel combination of triethylgallium (TEGa), trimethylindium, tertiarybutylarsine (TBAs), and trimethylantimony (TMSb); and AlGaAsSb with tritertiarybutylaluminum, TEGa, TBAs, and TMSb, as previously reported [2]. Diethyltellurium (50 ppm in H₂) and dimethylzinc (1000 ppm in H₂) were used as the *n*- and *p*-type doping sources, respectively. All layers were grown lattice matched to GaSb substrates at 575°C with V/III = 1.15 or 2.2 for GaInAsSb or AlGaAsSb, respectively. The growth rate of GaInAsSb was typically 0.7 nm/s, while that of AlGaAsSb was 0.2–0.4 nm/s. The reported compositions are based on Auger electron spectroscopy.

To evaluate the quality of GaInAsSb/AlGaAsSb quantum wells, a test structure consisting of a 0.1- μm -thick Al_{0.28}Ga_{0.72}As_{0.02}Sb_{0.98} buffer layer and five 15-nm-thick Ga_{0.87}In_{0.13}As_{0.12}Sb_{0.88} quantum wells separated by 20-nm-thick Al_{0.28}Ga_{0.72}As_{0.02}Sb_{0.98} barrier layers was grown. The double-crystal x-ray diffraction rocking curve shown in Figure 2-1 exhibits satellite peaks and interference fringes, indicating the high crystalline quality of the MQW structure. The lattice mismatch of -100 arc sec corresponds to $\Delta a/a = 9 \times 10^{-4}$. Photoluminescence (PL) spectra measured at 4 and 300 K of the MQW structure plotted in Figure 2-2 show emission at 1850 and 2048 nm, respectively. The full width at half-maximum of the 4-K PL is ~ 10 meV, which compares favorably with the value of 11–12 meV reported for quantum wells grown by molecular beam epitaxy (MBE) [3],[4].

The MQW diode laser structure was grown on an *n*-GaSb substrate with the following layers: 1- μm -thick *n*-Al_{0.6}Ga_{0.4}As_{0.05}Sb_{0.95} cladding layer, 0.3- μm -thick Al_{0.28}Ga_{0.72}As_{0.02}Sb_{0.98} confining layer, MQW active region consisting of four 15-nm-thick Ga_{0.87}In_{0.13}As_{0.12}Sb_{0.88} quantum wells separated by 20-nm-thick Al_{0.28}Ga_{0.72}As_{0.02}Sb_{0.98} barrier layers, 0.3- μm -thick Al_{0.28}Ga_{0.72}As_{0.02}Sb_{0.98} confining layer, 1- μm -thick *p*-Al_{0.6}Ga_{0.4}As_{0.05}Sb_{0.95} cladding layer, and 0.05- μm -thick *p*⁺-GaSb cap layer. The *n*-Al_{0.6}Ga_{0.4}As_{0.05}Sb_{0.95} cladding layer was doped to $\sim 6 \times 10^{15}$ cm⁻³ as determined by Hall measurements, while the *p*-Al_{0.6}Ga_{0.4}As_{0.05}Sb_{0.95} cladding layer was nominally undoped with a hole concentration of $\sim 2 \times 10^{18}$ cm⁻³. The nominally undoped confining layers with a residual hole concentration of $\sim 4 \times 10^{17}$ cm⁻³ were incorporated in the structure to reduce free-carrier absorption. Otherwise, the loss would be significant from the *p*-Al_{0.6}Ga_{0.4}As_{0.05}Sb_{0.95} cladding layer. The lattice mismatch of Al_{0.6}Ga_{0.4}As_{0.05}Sb_{0.95} cladding layers was $\Delta a/a = -9 \times 10^{-4}$. The interfaces between the 28 and 60% AlGaAsSb layers were graded to reduce the heterojunction resistance. Broad-area lasers 100 μm wide were fabricated by a standard photolithographic process [3], and devices were cleaved with various cavity lengths. Devices were tested under pulsed operation at room temperature with 400-ns pulses at a repetition rate of 1 kHz.

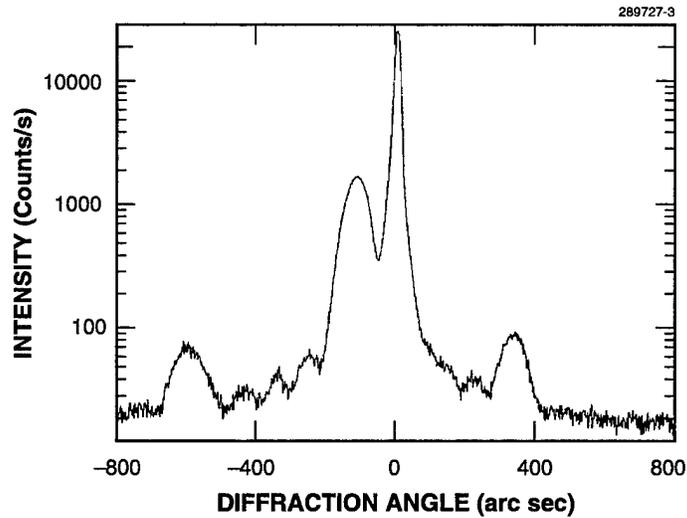


Figure 2-1. Double-crystal x-ray diffraction rocking curve of five-period $Ga_{0.87}In_{0.13}As_{0.12}Sb_{0.88}/Al_{0.28}Ga_{0.72}As_{0.02}Sb_{0.98}$ multiple-quantum-well (MQW) structure nominally lattice matched to GaSb substrate.

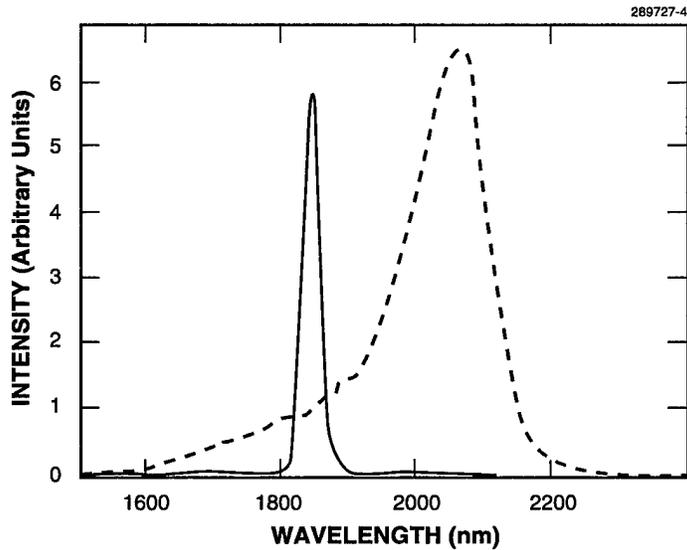


Figure 2-2. Photoluminescence spectra measured at 4 K (solid curve) and 300 K (dashed curve, $\times 10$) of five-period $Ga_{0.87}In_{0.13}As_{0.12}Sb_{0.88}/Al_{0.28}Ga_{0.72}As_{0.02}Sb_{0.98}$ MQW structure nominally lattice matched to GaSb substrate.

The dependence of threshold current density J_{th} on cavity length L is shown in Figure 2-3. As L increases from 500 to 2000 μm , J_{th} decreases from 2.1 to 1.2 kA/cm^2 , respectively. Figure 2-4 shows the emission spectrum from a 1.1-mm-long device at $I \sim 1.3 I_{th}$. It exhibits several longitudinal modes, as is

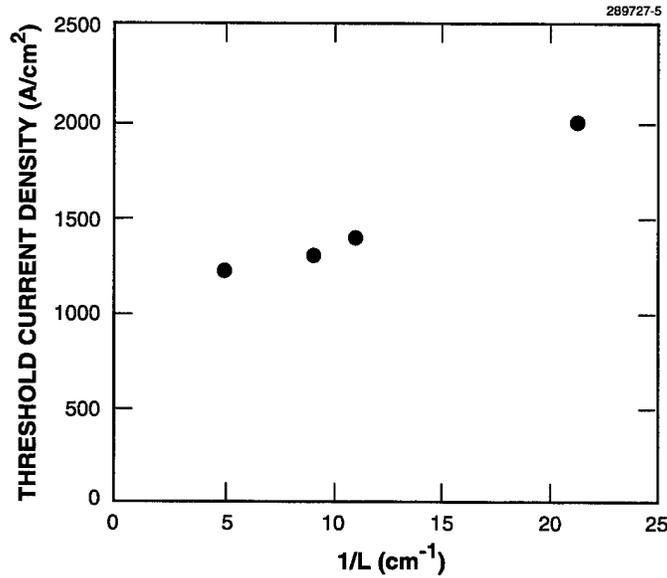


Figure 2-3. Threshold current density as a function of inverse cavity length of $\text{Ga}_{0.87}\text{In}_{0.13}\text{As}_{0.12}\text{Sb}_{0.88}/\text{Al}_{0.28}\text{Ga}_{0.72}\text{As}_{0.02}\text{Sb}_{0.98}$ MQW diode laser.

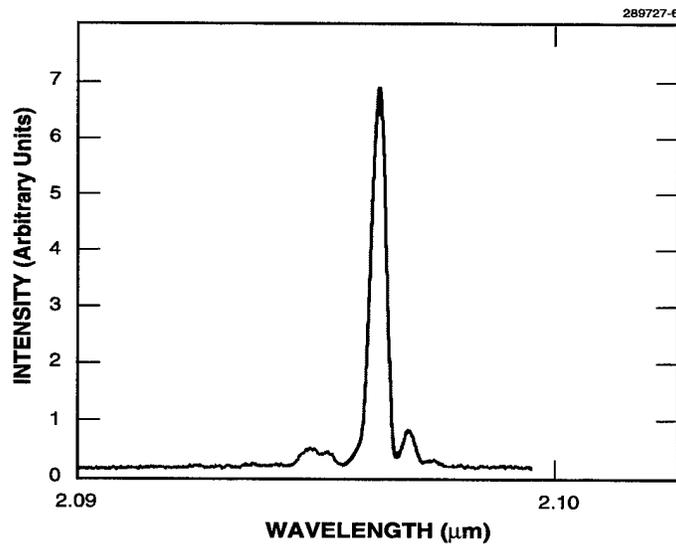


Figure 2-4. Emission spectrum of $\text{Ga}_{0.87}\text{In}_{0.13}\text{As}_{0.12}\text{Sb}_{0.88}/\text{Al}_{0.28}\text{Ga}_{0.72}\text{As}_{0.02}\text{Sb}_{0.98}$ MQW diode laser.

typically observed for broad-stripe lasers, and is centered at $\sim 2.1 \mu\text{m}$. The lasing wavelength is longer than the room-temperature PL peak of $2.06 \mu\text{m}$. The current-voltage curve of a 1-mm-long device indicates a series resistance of 2.5Ω .

The performance of these first GaInAsSb/AlGaAsSb MQW diode lasers is a significant improvement over our GaSb/AlGaAsSb double-heterostructure lasers, which had a pulsed J_{th} of 2.1 kA/cm^2 for a 1000- μm -long device. However, the values of J_{th} are much higher than those for GaInAsSb/AlGaAsSb strained MQW diode lasers emitting at $2.1 \mu\text{m}$ grown by MBE [3], which had J_{th} as low as 260 A/cm^2 . The higher J_{th} values reported here may be a result of the use of lattice-matched MQW active layers instead of biaxially compressed layers, as well as high oxygen levels in AlGaAsSb [5].

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2.2 HIGH THERMOELECTRIC FIGURES OF MERIT IN *p*-TYPE PbTe QUANTUM WELLS

Multiple-quantum-well structures composed solely of Pb-salt materials were found to have high Seebeck coefficients (up to $\sim 400 \mu\text{V/K}$), to grow with excellent structural quality, and to not have the autodoping problem of $\text{Bi}_y\text{Sb}_{1-y}/\text{PbTe}_{1-z}\text{Se}_z$ MQW structures. Consequently, Pb-salt MQW structures have provided an excellent medium for pursuing a basic investigation of thermoelectric superlattices. The $\text{Pb}_{1-x}\text{Eu}_x\text{Te}/\text{PbTe}$ materials system not only serves as a good vehicle for testing quantum-confinement effects on the Seebeck coefficient, but also can be used to indicate the magnitude of the thermal conductivity reduction expected in MQW superlattice structures due to phonon-interface scattering [6],[7]. Here, we report high-quality $\text{Pb}_{1-x}\text{Eu}_x\text{Te}/\text{PbTe}$ MQW structures grown by molecular beam epitaxy (MBE). A very thin, partial monolayer of BaF_2 inserted in the center of the $\text{Pb}_{0.927}\text{Eu}_{0.073}\text{Te}$ barrier was found to be a very effective acceptor dopant and to result in very high *p*-type thermoelectric power factors P_{F2D} and figures of merit $Z_{2\text{D}}T$. At 300 K, P_{F2D} values up to $\sim 160 \mu\text{Wcm}^{-1}\text{K}^{-2}$ have been measured and values of $Z_{2\text{D}}T > 1.5$ have been achieved for the *p*-type quantum wells. The measured 300- and 400-K thermoelectric properties of the quantum wells are many times better than those of the best bulk PbTe. For *p*-type PbTe quantum wells, we obtained $Z_{2\text{D}}T > 2.3$ at 400 K, the highest value obtained for any material.

The previously reported investigations of *n*-type PbTe MQW structures [8],[9] have recently been extended to *p*-type material. A number of structures composed of $\text{Pb}_{0.927}\text{Eu}_{0.073}\text{Te}/\text{PbTe}$ MQWs were grown by the previously described [9] MBE techniques. Hole charge carriers were provided to the *p*-type quantum wells by growing a layer of BaF_2 in the middle of the $\text{Pb}_{0.927}\text{Eu}_{0.073}\text{Te}$ barriers. In some initial experiments, thicker BaF_2 layers were grown to test a double-barrier concept where the first barrier (PbEuTe) provides high-quality interfaces to the quantum well and the second higher-energy barrier (BaF_2) provides better carrier confinement, so that the overall barrier thickness can be minimized. Wide

barriers are deleterious to realizing a high three-dimensional $Z_{3D}T$ because of high parasitic thermal conductance [7],[9]. Initial experiments involved placing a 2.0-nm-thick layer of BaF_2 in the center of the $Pb_{0.927}Eu_{0.073}Te$ barriers; however, we found that such layers degraded the crystal structure so severely that good thermoelectric properties were not realized. Nevertheless, Sun and Dresselhaus [10] have carried out detailed theoretical calculations on this new structure and find that the use of compound barriers is a good idea.

In subsequent experiments, a thin BaF_2 layer was used as an acceptor dopant only. Six $Pb_{0.927}Eu_{0.073}Te/PbTe$ MQW structures were grown with very thin BaF_2 layers placed in the barriers; their parameters are tabulated in Tables 2-1 and 2-2. The hole carrier concentration increased with BaF_2 layer thickness. Sample T-358 with a BaF_2 thickness $d_b = 0.11$ nm had a three-dimensional carrier concentration $p_{300} = 6.2 \times 10^{18} \text{ cm}^{-3}$ at 300 K, whereas T-368 with $d_b = 0.45$ nm had $p_{300} = 6.2 \times 10^{19} \text{ cm}^{-3}$. All of these samples had high Seebeck coefficients, ranging from 151 to 257 $\mu\text{V/K}$. The measured mobilities are much higher than is consistent with hole conduction in the $Pb_{0.927}Eu_{0.073}Te$ barrier region, so it is reasonable to assume that the carriers are confined to the $PbTe$ quantum wells. The two-dimensional carrier concentrations are obtained by assuming that the carriers are confined to the $PbTe$ quantum wells.

TABLE 2-1
Parameters of δ -Doped p -Type $Pb_{0.927}Eu_{0.073}Te/PbTe$
Multiple-Quantum-Well Structures

Sample No.	Sample Thickness (μm)	Number of Periods	300-K Seebeck Coefficient ($\mu\text{V/K}$)	Three-Dimensional Carrier Concentration		Carrier Mobility	
				300 K (cm^{-3})	77 K (cm^{-3})	300 K ($\text{cm}^2/\text{V s}$)	77 K ($\text{cm}^2/\text{V s}$)
T-329	5.25	224	+241	1.8×10^{19}	1.5×10^{19}	77	345
T-331	5.25	224	+229	1.3×10^{19}	1.3×10^{19}	110	400
T-371	5.58	238	+206	4.1×10^{19}	1.6×10^{19}	39	190
T-368	4.59	205	+151	6.2×10^{19}	2.4×10^{19}	35	200
T-358	5.25	220	+242	6.2×10^{18}	3.9×10^{18}	120	720
T-332	4.76	204	+257	4.1×10^{18}	2.3×10^{18}	120	770

TABLE 2-2
More Parameters of δ -Doped p -Type $\text{Pb}_{0.927}\text{Eu}_{0.073}\text{Te}/\text{PbTe}$
Multiple-Quantum-Well Structures

Sample No.	Thicknesses			Two-Dimensional Carrier Concentration	
	PbTe Well $d_w(\text{nm})$	BaF ₂ δ -Doped $d_b(\text{nm})$	Pb _{0.927} Eu _{0.073} Te Barrier $d_p(\text{nm})$	300 K (cm^{-3})	77 K (cm^{-3})
	T-329	1.91	0.22	19	2.0×10^{20}
T-331	1.91	0.22	19	1.6×10^{20}	1.6×10^{20}
T-371	2.07	0.22	20	4.5×10^{20}	1.6×10^{20}
T-368	1.97	0.45	19	6.7×10^{20}	2.7×10^{20}
T-358	1.90	0.11	19	6.8×10^{19}	4.3×10^{19}
T-332	1.88	0.22	19	4.9×10^{19}	2.8×10^{19}

To evaluate the PbTe MQW data, we have compared these results with bulk PbTe. Properties of the best bulk p -type PbTe samples [11],[12] known are listed in Table 2-3. These bulk materials were prepared from semiconductor-grade Pb and Te, grown by the Bridgman method, and were polycrystalline with large grain sizes. The low-concentration samples were undoped whereas the higher-concentration samples were doped with various impurities such as Ag, Au, and P. Seebeck coefficients at 300 K varied from +431 $\mu\text{V}/\text{K}$ at low carrier concentrations to +95 $\mu\text{V}/\text{K}$ at the highest concentration. At lower carrier concentrations, the highest 300-K carrier mobility was 950 $\text{cm}^2/\text{V s}$, which decreases to 780 $\text{cm}^2/\text{V s}$ at a carrier concentration of $1.5 \times 10^{19} \text{ cm}^{-3}$. Figure 2-5 shows a semilog plot of these S vs p data for bulk PbTe which are fit by a straight line given by the simple expression

$$S (\mu\text{V}/\text{K}) = +477 - 175 \log_{10}(p/10^{17} \text{ cm}^{-3}) \quad (2.1)$$

Except for changes in signs, this is exactly the same expression that fits the best bulk n -type data [9] for $n < 4 \times 10^{19} \text{ cm}^{-3}$. This is to be expected because the L conduction band pocket is the mirror image of the L valence band pocket and the electron effective mass is equal to the hole effective mass for the same carrier concentration. The effective mass of each L pocket increases with carrier concentration owing to band nonparabolicity. Notice that above $\sim 8 \times 10^{18} \text{ cm}^{-3}$, the data become dependent on the impurity. The difference in Seebeck coefficient between the Tl- and Na-doped bulk samples [13] is attributed in the literature to resonance-impurity scattering [14],[15] in the Tl-doped samples. From Equation (2.1) and the slow mobility change with carrier concentration, we get a maximum power factor $S^2 p e \mu_h = 24 \mu\text{W}/\text{cm K}^2$ at a concentration of $8 \times 10^{18} \text{ cm}^{-3}$, but using literature values for Na-doped PbTe a maximum power factor of $28 \mu\text{W}/\text{cm K}^2$ is obtained at $1.0 \times 10^{19} \text{ cm}^{-3}$. Using 20 $\text{mW}/\text{cm K}$ for the lattice thermal conductivity of PbTe, we calculate a maximum figure of merit $ZT_{\text{max}} = 0.35$ for p -type bulk PbTe at 300 K.

TABLE 2-3

Thermoelectric Properties of High-Quality *p*-Type Bulk PbTe Samples

Sample No.*	300-K Seebeck Coefficient <i>S</i> (μV/K)	300-K Power Factor (μW/cm K ²)	Carrier Concentration <i>p</i> (cm ⁻³)		Carrier Mobility μ (cm ² /V s)	
			300 K	77 K	300 K	77 K
3-69	+431	5.2	2.2 × 10 ¹⁷	2.1 × 10 ¹⁷	770	27 000
5-70H1B	+388	5.4	3.0 × 10 ¹⁷	3.3 × 10 ¹⁷	740	23 000
5-70H1A	+346	7.7	4.9 × 10 ¹⁷	5.4 × 10 ¹⁷	830	22 000
2-71H1	+213	22.7	3.3 × 10 ¹⁸	4.6 × 10 ¹⁸	950	15 000
1-72H1	+155	20.9	6.7 × 10 ¹⁸	9.7 × 10 ¹⁸	810	9000
12-71H1	+154	24.0	7.4 × 10 ¹⁸	1.1 × 10 ¹⁹	850	9100
1-72H6C	+117	21.4	1.25 × 10 ¹⁹	2.3 × 10 ¹⁹	780	4100
1-72H4B	+95	17.0	1.5 × 10 ¹⁹	2.8 × 10 ¹⁹	780	4800
T-376*	+170	31.2	1.7 × 10 ¹⁹	2.2 × 10 ¹⁹	385	1700

*All samples are Bridgman grown, except sample T-376, which is an epitaxial single layer of BaF₂-doped PbTe grown by molecular beam epitaxy.

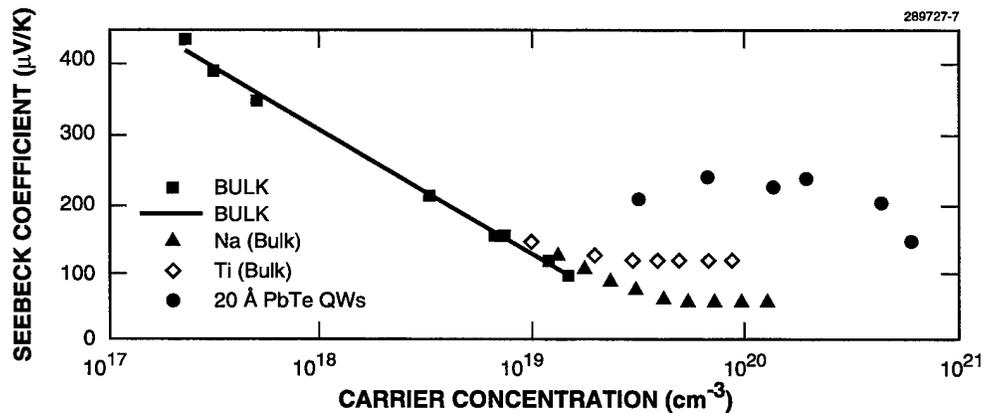


Figure 2-5. Seebeck coefficient vs hole carrier concentration for bulk *p*-type PbTe and *p*-type $Pb_{0.927}Eu_{0.073}Te$ /PbTe MQW structures. Data for Na- and Ti-doped bulk layers are also shown.

These results for bulk PbTe are compared in Figure 2-5 with S vs p data for the six BaF₂ δ -doped MQW structures and with data for an epitaxial layer of p -type PbTe. The MQW-structure data show a nearly constant value (in the range from high 10^{19} to 2×10^{20} cm⁻³) with increasing carrier concentration similar to that of Na- and Tl-doped bulk material. It is believed that this plateau is a consequence of the valence band structure of PbTe. Holes are predominantly in the L valence band pockets for hole carrier concentrations below mid- 10^{19} cm⁻³. Above 2×10^{20} cm⁻³, holes are predominantly in Σ valence band pockets. Constant-energy surfaces of the PbTe valence band extrema [16] are shown in Figure 2-6. The maximum extremum is located at the L point (light hole band) of the Brillouin zone and there are eight half or four whole ellipsoids. This is important for thermoelectricity because ZT is directly proportional to the number of ellipsoids (valleys) through the density-of-states effective mass. The next highest valence band extremum is located at the Σ point (heavy hole band) of the Brillouin zone and there are twelve whole ellipsoids, which is very favorable for high ZT . Thus, as the total hole carrier concentration increases, the percentage of (heavy) Σ holes relative to (light) L holes increases with the result that a relatively high Seebeck coefficient persists to extraordinarily high carrier concentrations. Thus, it is not necessary to invoke impurity resonance scattering to explain the high Seebeck coefficient in Tl-doped PbTe. The Tl-doped PbTe Seebeck coefficient of $120 \mu\text{V/K}$ at 2×10^{20} cm⁻³ can be calculated using a hole density-of-states effective mass of 1.2, which is reasonable in view of this valence-band structure. For the early literature on the second valence band in PbTe, see Refs. 17 and 18.

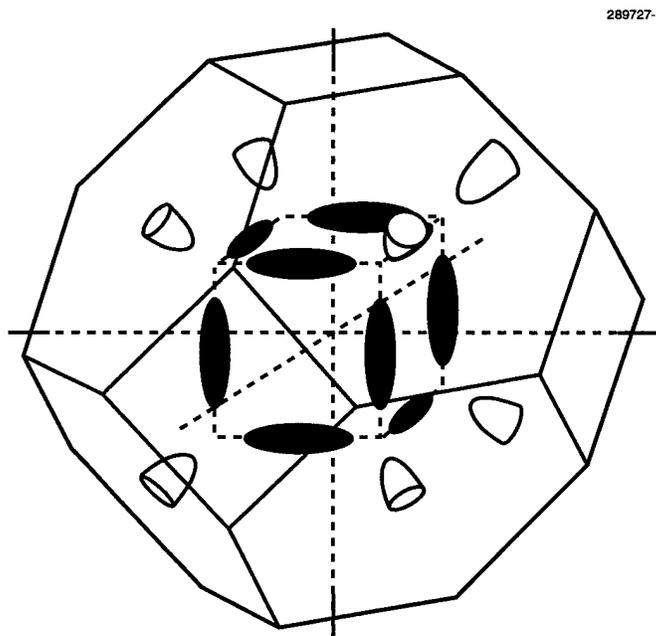


Figure 2-6. Constant-energy surfaces of the PbTe valence band in the Brillouin zone.

Our measured Seebeck coefficients for the MQW samples are approximately a factor of 2 larger than the Seebeck coefficients of bulk Tl-doped PbTe. At the very high carrier concentration of $2 \times 10^{20} \text{ cm}^{-3}$, we obtained a remarkably high Seebeck coefficient of $+240 \text{ } \mu\text{V/K}$. We believe that the 2 times increase in S (4 times increase in power factor $S^2\sigma$ and ZT) is primarily from quantum-well enhancement due to the increased density of states per unit volume of the quantum wells. Furthermore, measurements indicate that the hole carrier mobility can be at least as high as $110 \text{ cm}^2/\text{V s}$, which is roughly 4 times higher than that of bulk Tl-doped PbTe at this carrier concentration. We hypothesize that this 4 times mobility enhancement may be due primarily to the δ -doping. Mobility enhancement occurs owing to the suppression of impurity scattering in the quantum wells. At the $2 \times 10^{20} \text{ cm}^{-3}$ impurity concentration level, impurity scattering in the bulk material may contribute to some degradation of the carrier mobility, but since the impurities are placed in the middle of the barriers, the carriers in the undoped PbTe quantum wells are not subjected to impurity scattering. Thus, we believe a large carrier mobility enhancement occurs because of the δ -doping suppression of impurity scattering even though carrier-phonon and carrier-interface scattering does occur in the quantum wells. Detailed quantitative modeling of the p -type quantum-well superlattice structures in process may be able to sort out the relative contributions of the L valence band pocket and the Σ valence band pocket to the Seebeck coefficient and the hole carrier mobility.

Properties of an MBE-grown uniformly BaF_2 -doped single-layer PbTe sample are shown in Table 2-3. This sample has a power factor $31.2 \text{ } \mu\text{W/cm K}^2$ and a bulk $Z_{3D}T = 0.38$ at 300 K, which are values somewhat higher than those for any other p dopant in bulk PbTe. In Table 2-4 are listed the two-dimensional power factor $P_{\text{F2D}} = S^2pe\mu_h$ and thermoelectric figure of merit $Z_{2D}T$ for the six p -type PbTe MQW samples at 300 K, showing P_{F2D} values as high as $160 \text{ } \mu\text{W/cm K}^2$. The power factor vs hole concentration for these samples and for the best bulk p -type PbTe are displayed in Figure 2-7.

TABLE 2-4

Thermoelectric Properties at 300 K of p -Type $\text{Pb}_{0.927}\text{Eu}_{0.073}\text{Te/PbTe}$ Multiple-Quantum-Well Samples

Sample No.	Two-Dimensional Power Factor P_{F2D} ($\mu\text{W/cm K}^2$)	Electrical Conductivity σ_w (mho/cm)	Thermoelectric Figure of Merit* (Wells Only) $Z_{2D}T$
T-329	160	2700	1.5
T-331	150	2800	1.4
T-371	119	2800	1.1
T-368	88.5	3900	0.7
T-358	73	3900	0.9
T-332	63.5	960	0.8

*A literature value of the lattice thermal conductivity of 20 mW/cm K was assumed for the PbTe quantum wells and may be too high.

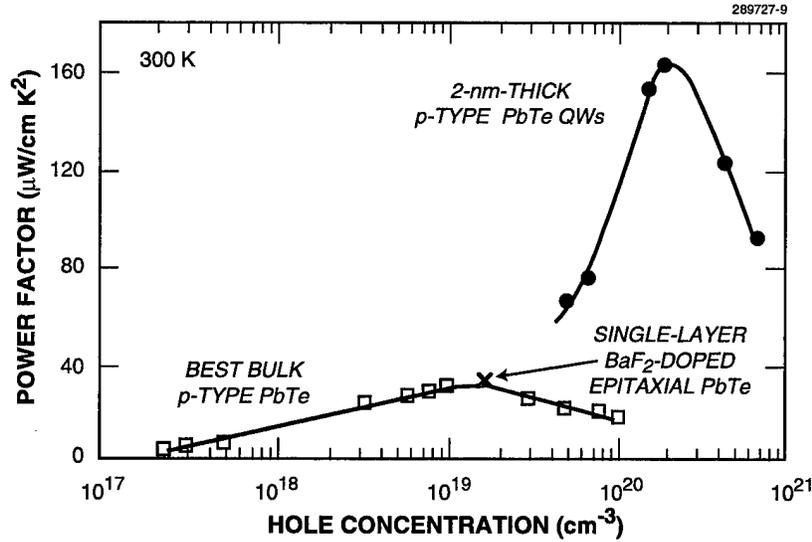


Figure 2-7. Thermoelectric power factor vs carrier concentration for the best *p*-type bulk PbTe samples, a single BaF₂-doped epitaxial PbTe layer, and *p*-type Pb_{0.927}Eu_{0.073}Te/PbTe quantum wells.

Power factors ($S^2\sigma$ for bulk or single layer and $S^2\sigma_w$ for quantum well) from Tables 2-3 and 2-4 are presented in Figure 2-7 as a function of the carrier concentration at 300 K. The bulk data show a very broad peak centered at a concentration $\sim 1.5 \times 10^{19} \text{ cm}^{-3}$, whereas the MQW data peak is much higher and narrower and centered at $\sim 2 \times 10^{20} \text{ cm}^{-3}$. The 2-nm-thick PbTe quantum wells with ~ 20 -nm-thick barriers have higher two-dimensional power factors than found for similar *n*-type quantum wells [8],[9] despite having a much lower carrier mobility. For the best sample, T-329, the power factor is $160 \mu\text{W}/\text{cm K}^2$, the highest reported to date for good thermoelectric materials.

The best thermoelectric properties at 300 K for the *n*- and *p*-type PbTe quantum wells investigated in the past two years are summarized in Table 2-5. Notice that we have achieved power factors in *p*-type quantum wells that are ~ 4 times the best bulk or single-layer value, and these power factors were achieved with a barrier thickness less than half as thick as that for the previously reported *n*-type [8],[9] MQW structures. Using the accepted bulk value of $20 \text{ mW}/\text{cm K}$ for the lattice thermal conductivity, we estimate $Z_{3D}T$ is as high as 0.24 and $Z_{2D}T = 1.5$ at 300 K. At 400 K, we get $Z_{2D}T > 2.3$. Since we expect interface scattering in the MQW structure is lowering the thermal conductivity, the actual ZT values may be considerably higher. We are in the process of measuring the thermal conductivity of these thin layers.

TABLE 2-5

Best Measured Power Factors and Estimated Overall Thermoelectric Figures of Merit $Z_{3D}T$ for 2.0-nm-thick PbTe Quantum-Well Structures at 300 K

Year	Carrier Type	Barrier Thickness (nm)	Power Factor Ratio $(S^2\sigma)_{2D}/(S^2\sigma)_{bulk}$	Estimated Thermoelectric Figure of Merit $Z_{3D}T^*$
1995	<i>n</i> -type	40.7	3.5	0.11
1996	<i>p</i> -type	19.3	4.0	0.24

*These estimated values may be low because the lattice thermal conductivity may be less than the assumed bulk PbTe values used in Table 2-4 due to phonon-interface scattering in the multiple-quantum-well superlattice structures.

The three-dimensional properties of these *p*-type quantum wells with an electrical conductivity of 275 mho cm^{-1} and a Seebeck coefficient S of $+241 \mu\text{V/K}$ at 300 K are intriguing. The composition of the best MQW structure is 9% PbTe, 1% BaF₂, and 90% Pb_{0.927}Eu_{0.073}Te. However, BaF₂ and Pb_{0.927}Eu_{0.073}Te have no charge carriers and essentially zero $Z_{3D}T$. Thus, despite the fact that only the 9% PbTe part of the sample is thermoelectrically active, the overall estimated $Z_{3D}T$ is 0.24 at 300 K.

In conclusion, the unusually high maximum power factor is believed to be the result of a combination of three factors: the quantum-well enhancement effect on the density of states per unit volume, the high density-of-states effective mass hole pocket of the Σ valence band, and δ -doping.

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REFERENCES

1. C. A. Wang and H. K. Choi, *Electron. Lett.* **32**, 1779 (1996).
2. C. A. Wang, *J. Cryst. Growth* **170**, 725 (1997).
3. H. K. Choi and S. J. Eglash, *Appl. Phys. Lett.* **61**, 1154 (1992).
4. W. Z. Shen, S. C. Shen, W. G. Tang, Y. Zhao, and A. Z. Li, *J. Appl. Phys.* **78**, 5696 (1995).
5. C. A. Wang, K. F. Jensen, A. C. Jones, and H. K. Choi, *Appl. Phys. Lett.* **68**, 400 (1996).
6. T. C. Harman, "Superlattice Structures Particularly Suitable for Use as Thermoelectric Cooling Materials," U.S. Patent No. 5,415,699 (16 May 1995).
7. G. D. Mahan, "Good Thermoelectrics," to be published in *Solid State Physics*, H. Ehrenreich and F. Spaepen, eds. (Academic, San Diego), p. 39; P. Hyldegaard and G. D. Mahan, in *Proceedings of the International Conference on Thermal Conductivity* (Plenum, New York, 1996).
8. L. D. Hicks, T. C. Harman, X. Sun, and M. S. Dresselhaus, *Phys. Rev. B* **52**, R10493 (1996).
9. T. C. Harman, D. L. Spears, and M. J. Manfra, *J. Electron. Mater.* **25**, 1121 (1996).
10. X. Sun and M. S. Dresselhaus, unpublished.
11. A. J. Strauss, private communication.
12. A. J. Strauss, *J. Electron. Mater.* **2**, 553 (1973).
13. B. F. Gruzinov, I. A. Drabkin, Yu. Ya. Eliseeva, E. Ya. Lev, and I. V. Nelson, *Sov. Phys. Semicond.* **13**, 767 (1979).
14. V. I. Kaidanov, S. A. Nemov, and Yu. I. Ravich, *Sov. Phys. Semicond.* **26**, 113 (1992).
15. S. D. Darchuk, L. A. Korovina, and F. F. Sizov, *Sov. Phys. Semicond.* **26**, 476 (1992).
16. H. Sitter, K. Lischka, and H. Heinrich, *Phys. Rev. B* **16**, 680 (1977).
17. R. S. Allgaier and B. B. Houston, Jr., *J. Appl. Phys.* **37**, 302 (1966).
18. N. V. Kolomoets, M. N. Vinogradova, E. Ya. Lev, and L. M. Sysoeva, *Sov. Phys. Solid State* **8**, 2337 (1967).

3. SUBMICROMETER TECHNOLOGY

3.1 THERMAL CONDUCTIVITY CHARACTERIZATION OF PECVD MICROBOLOMETER MEMBRANE MATERIALS

Thin films are important elements in microelectronics, optoelectronics, and optics. In microelectromechanical systems, measurement and control of the thermal conductivity of a thin film can be critical for some applications. In addition, because thermal conductivity is sensitive to the microstructure of solids, changes in measured thermal conductivity may correlate to variations in mechanical strength or permeability not readily detectable by other methods. Recently, considerable effort has been devoted to uncooled infrared focal plane arrays for both military and civilian applications [1]. The most common detector design for these arrays is based on a free-standing membrane microbolometer. One of the most critical material properties affecting the performance of this sensor is thermal conductivity of the membrane. Here, we show how a new method for measuring thermal conductivity of thin films has been used to aid in the optimization of plasma-enhanced chemical vapor deposition (PECVD) thin films for the microbolometer application.

In order to evaluate the thermal characteristics of a wide variety of membrane materials, a prototype photoacoustic thermal conductivity measurement instrument was obtained from Inrad. Although many other methods have been reported for measuring thin films [2], this method is ideally suited for design and testing of new materials. This apparatus exposes the sample to an intensity-modulated beam of light that periodically heats the surface. The instrument then measures the amplitude of the acoustic wave that is created near the surface of the sample owing to the periodic expansion and contraction of the gas layer adjacent to the surface, as a result of the periodic change in the surface temperature.

The signal obtained in a single measurement is proportional to the thermal resistance of the tested film if the thermal conductivity of the substrate is high compared to the thermal conductivity of the film. The modulation frequency is selected such that the film is "thermally thin," and the substrate is "thermally thick," or $d_f \ll (\omega_0/k_f)^{-1/2}$, $d_s \gg (\omega_0/k_s)^{-1/2}$, where $d_{f,s}$ is the thickness of the film or substrate, ω_0 is modulation frequency, and $k_{f,s}$ is the thermal diffusivity of the film or substrate, respectively.

The thermal resistance of a film normal to the surface is defined as

$$R = \Delta T/Q \quad , \quad (3.1)$$

where ΔT is the temperature difference between the two film surfaces and Q is heat flow density. The measured thermal resistance R relates to the thermal conductivity λ of the film by a simple equation:

$$R = d/\lambda + R_{\text{int}} \quad , \quad (3.2)$$

where d is the physical thickness of the film, and R_{int} is the thermal resistance of the interface between the thin film and the substrate. It is assumed that the film is uniform; otherwise, λ represents average thermal conductivity. One-dimensional heat flow is assumed in Equations (3.1) and (3.2), which holds true in most situations.

In order to ensure complete and consistent absorption of light at the surface of the sample regardless of the substrate or thin film being measured, the sample is coated prior to measurements with a light-absorbing and highly thermally conductive coating. The additional thermal resistance of the coating is canceled out in the differential technique. By using this method, the signal S that is proportional to the temperature modulation δT at the sample surface is

$$S \propto \delta T \propto Q/[\lambda_s(\omega_0/k_s)^{1/2}] + QR_f + QR_c \quad , \quad (3.3)$$

where R_c is the thermal resistance of the light-absorbing coating. The first term in Equation (3.3) is the contribution of the substrate, whereas the second and the third ones are caused by the film under test and the coating, respectively. If a second measurement is made in the area in which the film has been removed, this signal does not include the QR_f term and, therefore, the difference between the two signals is proportional to the R_f sought.

Prior to using the instrument to evaluate PECVD films, we measured the thermal conductivity of several types of thin films of technological importance. Figure 3-1 plots the thermal resistance as a function of film thickness for a thermally grown oxide and an electron-beam-evaporated oxide measured at room temperature. The slope of the linear best fit is $1/\lambda$ and its intercept is R_{int} [Equation (3.2)]. The linear fit of the data yields a thermal conductivity for the thermal oxide of 1.065 W/mK, which is very close to the published value for bulk amorphous silicon dioxide. Significantly, the electron-beam-evaporated oxide has a much lower thermal conductivity (0.618 W/mK) consistent with a less dense material. Notice that there is a non-negligible thermal resistance at the oxide/silicon interface for both types of oxides.

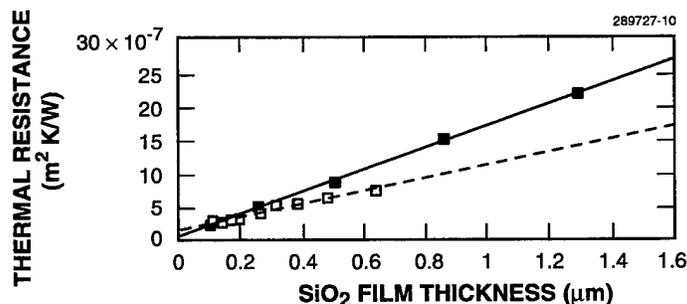


Figure 3-1. Measured thermal resistances of silicon dioxide films formed by electron-beam evaporation (filled squares) and thermal oxidation (open squares). Lines show linear fit resulting in values of thermal conductivities of 0.618 and 1.065 W/mK for evaporated and thermally grown films, respectively.

Another glassy material, silicon nitride, has been used in the formation of membranes in x-ray lithography, microelectromechanical devices, and uncooled infrared detectors because of its high tensile strength. In the latter application, it has been the material of choice. However, the nitride membrane must not only be strong but must have a low thermal conductivity as well [1] for the bolometer. Figure 3-2 plots the thermal resistance of sputter-deposited silicon nitride thin films. The slope yields $\lambda = 1.20$ W/mK. The small negative intercept is not yet fully explained, but is apparently an artifact of the deposition process and the resultant layered structure of the films. Note that the value of 1.2 W/mK for silicon nitride is close to that reported recently using the 3ω technique [3]–[5] but much lower than the value of 5 W/mK listed for bulk silicon nitride [6].

The main goal in designing an alternative PECVD membrane material is to reduce the material's thermal conductivity below that of silicon nitride. In general, polymers have thermal conductivities an order of magnitude lower than glassy materials such as silicon nitride and silicon oxide. However, there are many other design considerations for the membrane material which polymers do not satisfy.

In order to examine the lower limit of thermal conductivity, we measured the thermal resistances of two commercially available spin-applied polymers: polymethylmethacrylate (PMMA) and hard-baked photoresist (novolac based). Using the photoacoustic method, we measured thermal conductivities of 0.14–0.18 W/mK for these polymers, respectively, almost an order of magnitude lower than those of the silicon nitride or oxide. In Figure 3-3, two sets of measurements are plotted to indicate the reproducibility of the technique. The open circles represent PMMA samples that were coated and immediately measured. The closed circles are the values obtained on the same samples several days later. The slopes yield values of thermal conductivity of 0.135 and 0.147 W/mK, a difference of less than 10%. This compares reasonably well with the bulk value of 0.21 W/mK for PMMA [7]. Note in Figure 3-4 that much thicker films were evaluated for this polymer but still within the linear portion of the photoacoustic response. This too compared reasonably well with bulk values of 0.25 W/mK for casting-grade phenolic resins [7].

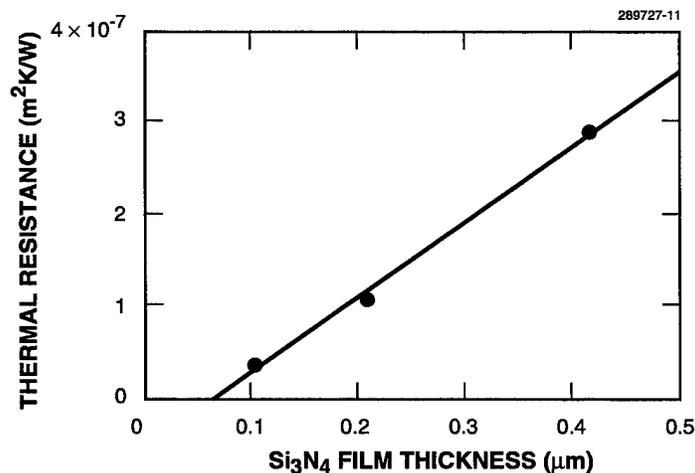


Figure 3-2. Measured thermal resistances of sputtered silicon nitride films of various thicknesses. Line shows linear fit resulting in a value of thermal conductivity of 1.20 W/mK.

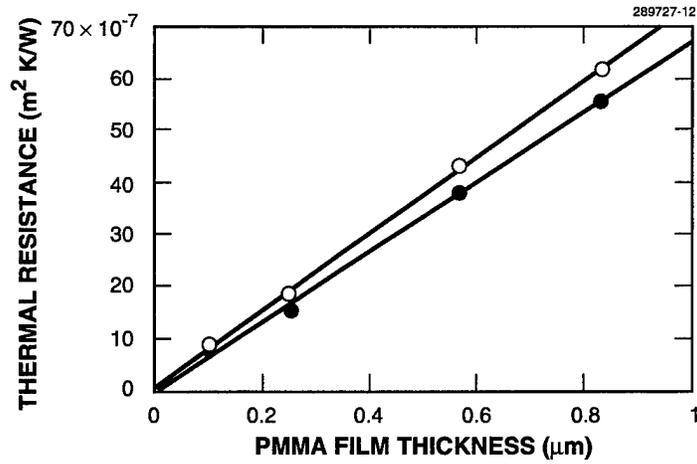


Figure 3-3. Measured thermal resistances of spin-applied polymethylmethacrylate (PMMA) films of various thicknesses measured just after application (open circles) and several days later (closed circles). The resulting thermal conductivity values were 0.135 and 0.147 W/mK, respectively.

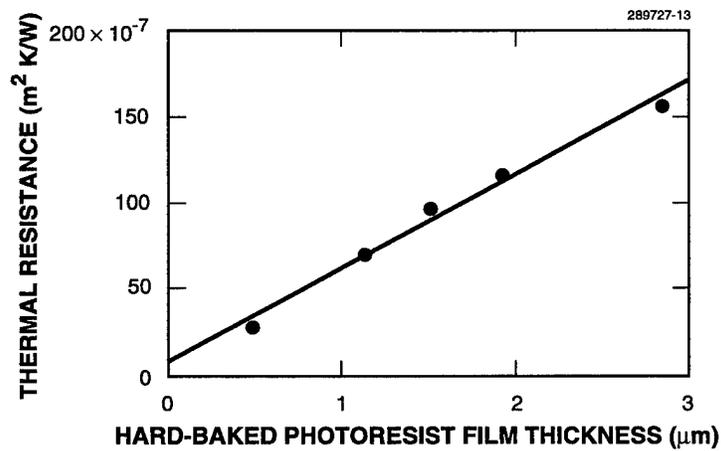


Figure 3-4. Measured thermal resistances of hard-baked novolac-based photoresist films. Line shows linear fit resulting in a value of thermal conductivity of 0.184 W/mK. Note that the films are much thicker than the PMMA films of Figure 3-3.

We examined many different kinds of PECVD thin films as alternative membrane materials. Besides low thermal conductivity, there are many other criteria for designing an optimum material such as high optical absorption in the range 8–14 μm , excellent mechanical strength, and process compatibility issues such as chemical resistance and adhesion. Figures 3-5 and 3-6 show examples of thermal resistance as a function of film thickness for two different plasma-deposited films that have been partially optimized with respect to the aforementioned criteria. These materials were deposited in a parallel-plate, rf-powered

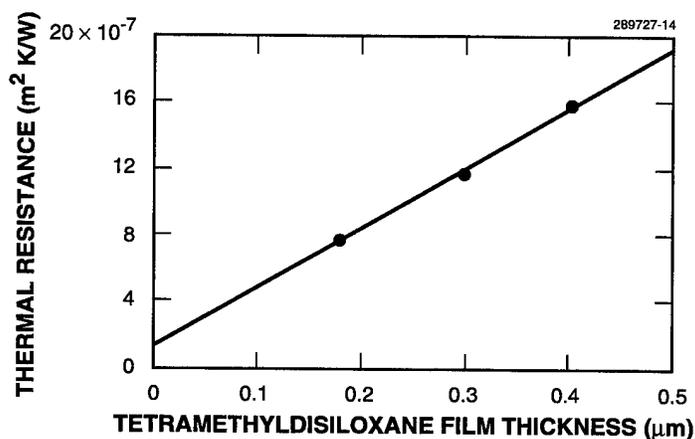


Figure 3-5. Measured thermal resistances of plasma-deposited organosilicon films. Line shows linear fit resulting in a value of thermal conductivity of 0.287 W/mK, lower than that for oxide but higher than for the polymers of Figures 3-3 and 3-4.

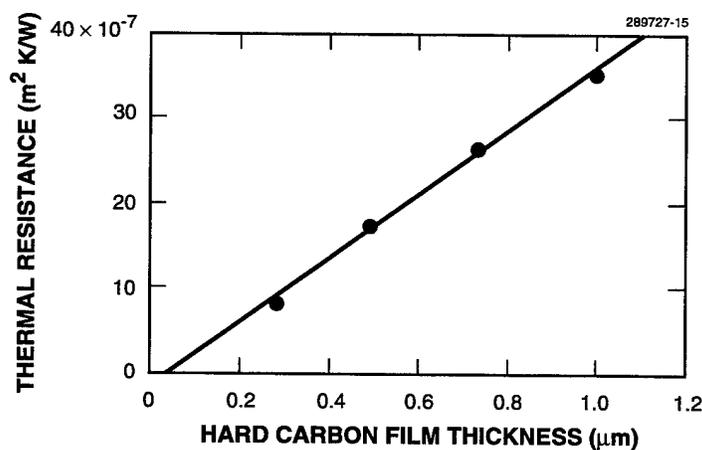


Figure 3-6. Measured thermal resistances of plasma-deposited hard carbon films. Line shows linear fit resulting in a value of thermal conductivity of 0.268 W/mK.

plasma deposition system [8],[9]. Figure 3-5 plots the thermal resistance of films deposited from an organosilicon compound, tetramethyldisiloxane. This material has physical and optical properties intermediate between those of silicon oxide and organic polymers as determined by ellipsometry and Fourier transform infrared spectroscopy. Indeed, the thermal conductivity of these films (0.287 W/mK) is a factor of 4 lower than that of silicon oxide or nitride, and ~ 2 times higher than that of PMMA. For comparison, the bulk value for a similar silicon-containing polymer, poly(dimethylsiloxane), is 0.22 W/mK [7]. Figure 3-6 plots thermal resistance vs film thickness for a plasma-deposited amorphous carbon material formed under conditions of high ion bombardment energies (300 V). These conditions yield a very hard film as measured by a scratch test. Note that the thermal conductivity is a factor of 2 higher than that of hard-baked photoresist. This result is in agreement with a model where mechanical hardness relates to density, and therefore to thermal resistance.

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REFERENCES

1. P. Finney, *Sensors* **13**, 36 (1996).
2. K. E. Goodson and M. I. Flik, *Appl. Mech. Rev.* **47** (3), 101 (1994).
3. D. G. Cahill, *Rev. Sci. Instrum.* **61**, 802 (1990).
4. D. G. Cahill, H. E. Fischer, T. Klitsner, E. T. Swartz, and R. O. Pohl, *J. Vac. Sci. Technol. A* **7**, 1259 (1989).
5. S.-M. Lee and D. G. Cahill, to be published in *J. Appl. Phys.*
6. Y. S. Touloukian, R. W. Powell, C. Y. Ho, and P. G. Klemens, eds., *Thermal Conductivity: Non-metallic Solids*, Vol. 2 of *Thermophysical Properties of Matter* (IFI/Plenum, New York, 1970), p. 662.
7. Y. Yang, in *Physical Properties of Polymers Handbook*, J. E. Mark, ed. (AIP, Woodbury, N.Y., 1996), p. 111.
8. M. W. Horn, S. W. Pang, and M. Rothschild, *J. Vac. Sci. Technol. B* **8**, 1493 (1990).
9. M. W. Horn, M. Rothschild, B. E. Maxwell, R. B. Goodman, and L. M. Eriksen, *Appl. Phys. Lett.* **68**, 179 (1996).

4. HIGH SPEED ELECTRONICS

4.1 SELF-ALIGNED PSEUDOMORPHIC HEMT WITH A LOW-TEMPERATURE-GROWN GaAs GATE INSULATOR

A GaAs-based pseudomorphic high-electron-mobility transistor (pHEMT) with a strained InGaAs channel and AlGaAs gate has demonstrated not only lower gate leakage current but also higher speed than conventional metal-semiconductor field-effect transistors (MESFETs) and has become the device of choice for GaAs complementary logic circuits [1]. Even with a side-bandgap AlGaAs gate layer, the turn-on voltage of the Schottky-barrier gate is still relatively small. The low turn-on voltage limits the logic level and the noise margin, and the gate leakage current under forward bias also contributes a significant portion of the power consumption in a complementary logic circuit. It has been shown that replacing AlGaAs with low-temperature-grown (LTG) GaAs as the gate insulator produced a higher gate turn-on voltage in complementary metal-insulator-semiconductor FETs (MISFETs) [2]. The purpose of this work is to explore the feasibility of using LTG GaAs as the gate insulator in a pHEMT thereby combining the advantages of a very low gate current and high speed in a single device suitable for integrated circuits.

All the layers were grown by molecular beam epitaxy on 3-in. semi-insulating GaAs substrates. As shown in Figure 4-1, the layer structure consists of a 2000-Å-thick GaAs buffer, a 10-Å-thick GaAs layer doped to $3.5 \times 10^{17} \text{ cm}^{-3}$, a 30-Å-thick GaAs spacer, and a 130-Å-thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ channel used to adjust the threshold voltage [3]. The growth temperature was 630°C for all the layers except for the LTG GaAs, which was grown at 200°C and then annealed at 630°C for 10 min before growing the AlAs barrier and GaAs cap on top. The AlAs barriers are needed to prevent the diffusion of the As precipitates in the LTG GaAs layer during implant annealing [4]. Because of the relatively high growth temperature, the actual In content in the InGaAs channel was slightly lower than the designed 20%.

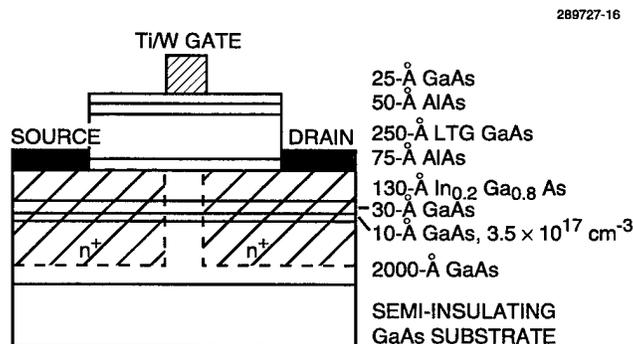


Figure 4-1. Cross-sectional view of the low-temperature-grown (LTG) GaAs pseudomorphic high-electron-mobility transistor.

The fabrication started with the deposition of 1500-Å-thick Ti/W gate metal by sputtering. The 0.5- μm gate was defined by optical lithography and then patterned by reactive ion etching. Next, the source and drain n^+ regions were implanted with Si using the Ti/W gate metallization as the self-aligned mask. The implant energy and the dose for the n^+ regions were 80 keV and $4.0 \times 10^{13} \text{ cm}^{-2}$, respectively. After activation annealing the source and drain contact regions were defined in photoresist and the gate insulator layers were etched in the exposed ohmic regions to expose the InGaAs channel. Then the Ni/Ge/Au ohmic-contact metal was evaporated and defined by liftoff using the same photoresist that was patterned for etching. The ohmic contact was formed by alloying in a rapid thermal annealing system. Finally, the devices were isolated by proton implant and the Ti/Au probing pads were deposited by liftoff. The gate length and width of the LTG-GaAs pHEMT were 0.5 and 100 μm , respectively, and the spacing between the source and drain ohmic contacts was 2.5 μm .

Figure 4-2(a) shows the typical drain current vs drain voltage ($I_{\text{ds}}-V_{\text{ds}}$) characteristics of an LTG-GaAs pHEMT. It is normally off with a threshold voltage V_t of 0.63 V. The device has a sharp pinch-off with a subthreshold slope of 116 mV/decade, and it shows no sign of gate conduction even at 3 V of forward gate bias. The maximum I_{ds} is 390 mA/mm of gate width measured at a gate bias $V_{\text{gs}} = +3$ V. As shown in Figure 4-2(b), the transconductance g_m peaks at $V_{\text{gs}} = 1.4$ V with a value of 333 mS/mm. The low output conductance in the saturation regime, 9.1 mS/mm at $V_{\text{gs}} = 1.4$ V, suggests that the conducting electrons are well confined for this submicron-gate-length self-aligned pHEMT. The K factor, defined as $I_{\text{ds}} = K(V_{\text{gs}} - V_t)^2$, was 360 mA/V² mm. Even though in an LTG-GaAs pHEMT the conducting channel is separated from the gate metal by the LTG-GaAs insulator, the K factor is comparable to self-aligned MESFETs in which the gate metal is placed directly on the channel [5],[6]. The drawback of having the gate metal away from the channel in the LTG-GaAs pHEMT is probably compensated by the higher mobility and better charge confinement in the InGaAs channel.

The average sheet resistance of the implanted n^+ regions is 430 Ω/square , and the specific contact resistance for the ohmic contact is in the low $10^{-6} \Omega \text{ cm}^2$ range. The relatively high sheet resistance indicates that the implant and the annealing schedules need to be improved. Because of the self-aligned configuration and a short source-drain spacing, a low drain-source on-resistance of 1.6 $\Omega \text{ mm}$ and a knee voltage of only 0.7 V at 390 mA/mm are obtained. Even with the relatively high sheet resistance, the drain-source on-resistance and the knee voltage are already lower than those in a conventional recessed-gate pHEMT with 0.1- μm gate length [7].

As a result of the high-resistivity LTG-GaAs gate insulator, the gate current I_{gs} measures only 5 nA/ μm^2 at 1 V of forward gate bias. The gate forward turn-on voltage, defined as the gate voltage at which $I_{\text{gs}} = 1 \mu\text{A}/\mu\text{m}^2$, is 1.78 V, which is slightly higher than that of the 1- μm -gate-length heterostructure insulated gate (HIG) FET with an AlGaAs gate layer [3]. The 9.8-V reverse breakdown voltage is high considering that there is no lightly doped drain region which is necessary for a self-aligned MESFET [8] and it is also higher than the 6 V of the HIGFET used for RF power amplifiers [9]. Without the use of an AlGaAs or an LTG-GaAs buffer layer, the off-state drain-source leakage current, measured at $V_{\text{gs}} = 0$ V and $V_{\text{ds}} = +2$ V, is only 60 nA for a 100- μm -wide LTG-GaAs pHEMT.

For a 100- μm -wide LTG-GaAs pHEMT with 0.5- μm gate length, the unity current gain cutoff frequency f_T obtained from measured scattering parameters was 14.3 GHz at $V_{\text{ds}} = 3$ V and $V_{\text{gs}} = 1.4$ V. The estimated electron mobility in the channel is 4100 $\text{cm}^2/\text{V s}$ with a sheet charge density of $2.5 \times 10^{12} \text{ cm}^{-2}$.

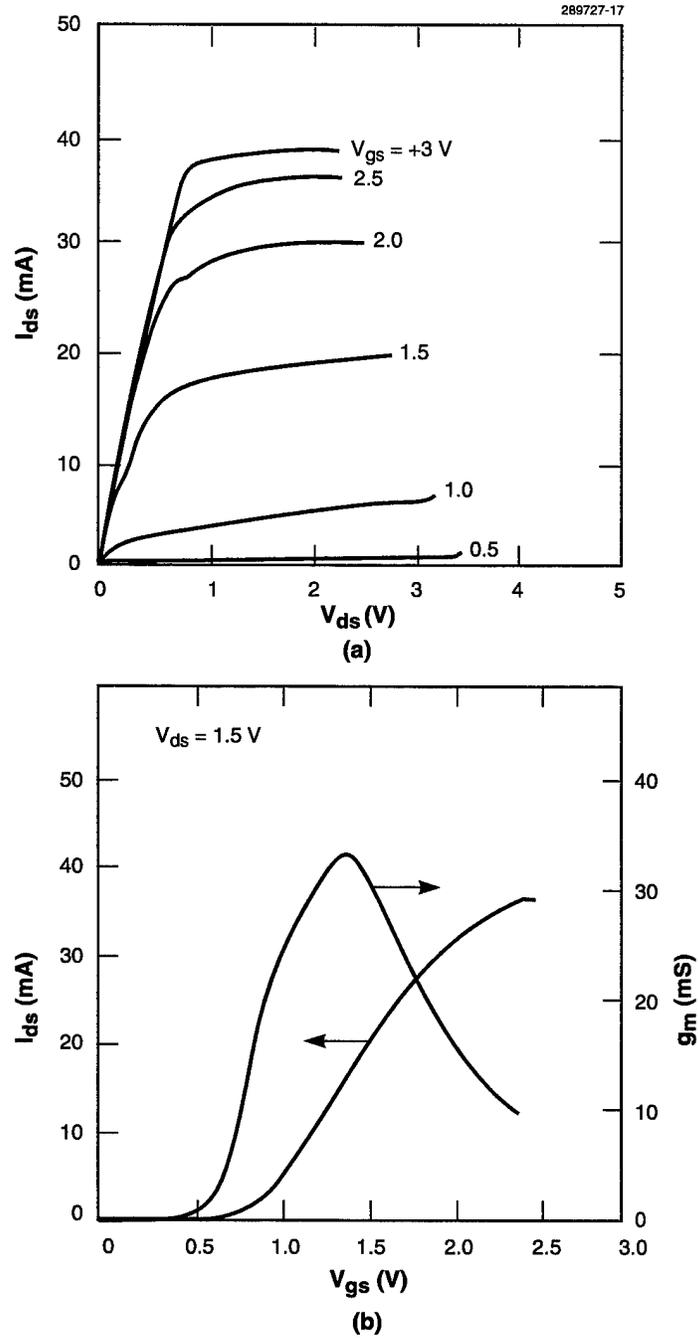


Figure 4-2. DC characteristics of the LTG-GaAs metal-insulator-semiconductor field-effect transistor with 100- μm -wide gate: (a) I_{ds} - V_{ds} with top $V_{gs} = 3$ V, and (b) I_{ds} and g_m as a function of V_{gs} at $V_{ds} = 1.5$ V.

A pHEMT with an LTG-GaAs gate insulator is reported for the first time. The significance of this work is the demonstration that LTG GaAs can replace AlGaAs in a complicated device structure, such as a pHEMT. Even without optimization, the potential benefit of using the LTG GaAs has become obvious. The LTG-GaAs pHEMT is normally off and no gate recess is needed. The low gate current, sharp pinch-off, and low knee voltage along with a high g_m and K factor make it ideal for low-voltage direct-coupled digital circuit applications. In addition, because of the high drain current and breakdown voltage, the normally off LTG-GaAs pHEMT is also suitable for low-voltage, high-efficiency power amplifiers with a single supply for wireless-communication applications. The material growth and fabrication can be further improved to reduce the gate leakage current and increase the mobility in the InGaAs channel. Complementary LTG pHEMTs are possible based on the similarities between the n -channel device reported here and complementary HIGFETs and LTG-GaAs MISFETs [2].

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REFERENCES

1. D. E. Grider, P. P. Ruden, J. C. Nohava, I. R. Mactaggart, J. J. Stronczer, T. E. Nohava, and S. S. Swirhun, *IEEE International Electron Devices Meeting Technical Digest* (IEEE, New York, 1991), p. 235.
2. C. L. Chen, L. J. Mahoney, K. B. Nichols, and E. R. Brown, *Electron. Lett.* **32**, 407 (1996).
3. J. K. Abrokwhah, J. H. Hwang, W. Ooms, C. Shurboff, J. A. Hallmark, R. Lycero, J. Gilbert, B. Bernhardt, and G. Hansell, *IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest* (IEEE, New York, 1993), p. 127.
4. C. L. Chen, L. J. Mahoney, K. B. Nichols, M. J. Manfra, E. R. Brown, P. M. Nitishin, K. M. Molvar, B. F. Gramstorff, and R. A. Murphy, *J. Vac. Sci. Technol. B* **14**, 1745 (1996).
5. J. Mikkelsen, *IEEE International Electron Devices Meeting Technical Digest* (IEEE, New York, 1991), p. 231.
6. M. R. Wilson, D. E. Chasson, B. S. Krongard, R. W. Rosenberry, N. A. Shah, and B. M. Welch, *IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest* (IEEE, New York, 1993), p. 189.
7. K. L. Tan, R. M. Dia, D. C. Streit, T. Lin, T. Q. Trinh, A. C. Han, P. H. Liu, P. D. Chow, and H. C. Yen, *IEEE Electron Device Lett.* **11**, 585 (1990).
8. Y. Kitaura, K. Nishihori, Y. Tanabe, M. Mihara, M. Yoshimura, T. Nitta, Y. Kakiuchi, and N. Uchitomi, *IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest* (IEEE, Piscataway, N.J., 1996), p. 245.
9. E. Glass, J. Abrokwhah, R. Lucero, E. Spears, J. Rollman, J-H. Huang, B. Bernhardt, and W. Ooms, *IEEE International Microwave Symposium Digest* (IEEE, Piscataway, N.J., 1996), p. 1083.

5. MICROELECTRONICS

5.1 128 × 128-PIXEL CHARGE-COUPLED DEVICE IMAGER AND CAMERA ELECTRONICS

A 128 × 128-pixel charge-coupled device (CCD) imager and the corresponding camera electronics have been developed for use in a visible wavefront sensor. The wavefront sensor is one of the components in an adaptive optics system that is being developed. This report describes the performance and features of the CCD imager and camera electronics.

Figure 5-1 shows a schematic and photograph of the 128 × 128-pixel CCD imager, which features high sensitivity and low noise at high frame rate. This imager has a split frame-transfer architecture that enables 16 readout amplifiers to be located around the chip and reduces the time required to transfer an image into the frame store regions. Each of the 16 ports is responsible for output of a 16 × 64-pixel section of the full 128 × 128-pixel image. The multiple output ports reduce the pixel frequency per port for a given frame rate, thereby reducing readout noise. The readout noise at 1 MHz has been measured at $4.5 e^-$ rms while at the maximum pixel rate of 4 MHz the noise is $7.5 e^-$. Back illumination of the CCD imager [1] results in sensitive light detection over the visible spectrum with quantum efficiencies as high as 90% in the 500- to 700-nm band. The CCD imagers also contain an integrated electronic shutter [2] with switching times of ~ 50 ns and an extinction ratio value (signal detected shutter opened to shutter closed) of 10^4 for wavelengths below 540 nm.

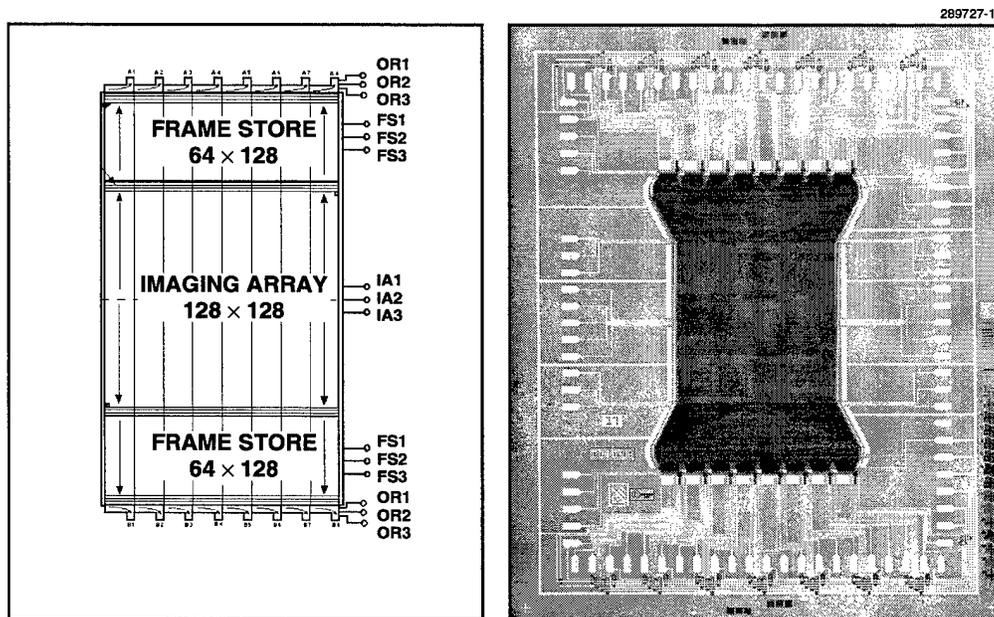


Figure 5-1. Schematic and photograph of a 128 × 128-pixel charge-coupled device imager with a split frame architecture and 16 readout amplifiers.

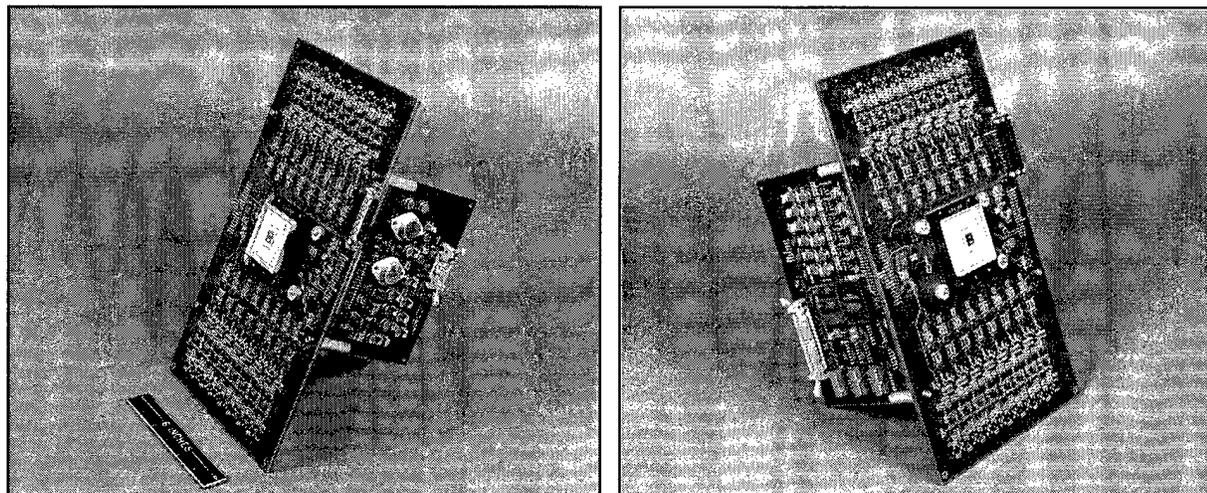


Figure 5-2. Photographs of multilayer printed circuit boards that constitute the electronic board set. Not shown in this particular view is the timing board.

Figure 5-2 shows photographs of the camera system that uses the CCD imager just described. This system consists of a 128×128 -pixel back-illuminated CCD imager and three multilayer printed circuit boards. The board set provides all the digital timing and analog drive and post-processing circuitry necessary to operate the CCD. The board that contains the CCD also has 16 analog circuit chains (one for each of the CCD output ports) used for amplifying the raw video signal and removing the reset noise. The analog chain also includes low-pass filtering that has three selectable bandwidths optimized for frequencies of 1, 2, and 4 MHz. Another board contains the state machine and addressable memory that creates all the necessary timing information to operate the CCD under various conditions. The last board has the analog level shifters needed for translating the digital signal from the timing board into clock levels appropriate for the CCD imager. The camera system operates at 700 frames per second at a read noise of $4.5 e^-$ rms and has a maximum frame rate of 2500.

The camera system has several modes of operation. These modes include combinations of row and column binning to increase the frame rate, and signal and image array flushing to provide very short integration times. The state machine that generates the timing sequences is a programmable logic device (PLD). The PLD chip addresses a set of EPROMs that produce the TTL signals required to operate the CCD imager and also to interface with the user electronics. The camera system has a dynamic range of 66–72 dB or an equivalent digital dynamic range of 11–12 bits. The dynamic range of the system is limited by the track-and-hold circuit used to do the correlated-double sampling.

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REFERENCES

1. C. M. Huang, B. E. Burke, B. B. Kosicki, R. W. Mountain, P. J. Daniels, D. C. Harrison, G. A. Lincoln, N. Usiak, M. A. Kaplan, and A. R. Forte, *IEEE Symposium on VLSI Technology Systems and Applications* (IEEE, New York, 1989), p. 98.
2. R. K. Reich, R. W. Mountain, W. H. McGonagle, J. C. M. Huang, J. C. Twichell, B. B. Kosicki, and E. D. Savoye, *IEEE Trans. Electron Devices* **40**, 1231 (1993).

6. ANALOG DEVICE TECHNOLOGY

6.1 NEW SELF-ALIGNED PLANAR RESONANT-TUNNELING DIODE PROCESS FOR MONOLITHIC CIRCUITS

The high-speed nonlinear properties of resonant-tunneling diodes (RTDs) enable a number of extremely fast circuits, including standard logic elements of reduced complexity as compared with transistor logic families. To reach the promised potential of these circuits for low-power operation at clock frequencies of many gigahertz, tight control over the peak current of individual RTDs is required. This translates into control over both the wafer uniformity of the RTD layers and the effective areas of the individual RTDs. This report describes the results of the first test wafers fabricated using a new process designed to improve the control over the effective area by using a self-aligned implant method to define the RTDs, and incorporating a contact to the buried terminal, effectively creating a planar structure.

RTDs are based on vertical current flow through an epitaxial layer structure. A typical structure, and the one we report on here, is grown by molecular beam epitaxy (MBE) on semi-insulating (SI) GaAs and consists of an $\text{In}_x\text{Ga}_{x-1}\text{As}$ layer sandwiched between two AlAs layers, forming a quantum well that gives rise to the nonlinear current-voltage (I-V) relationship. An RTD I-V curve, as shown in Figure 6-1, includes a region of negative differential resistance (NDR). The devices are characterized by a peak current (the maximum current below the NDR region), a valley current (the minimum current above the NDR region), and the voltages associated with those currents. Individual RTDs are created by restricting current flow to limited areas, and their I-V and capacitance properties depend on both the local properties of the epitaxial layers and the effective area of the RTD.

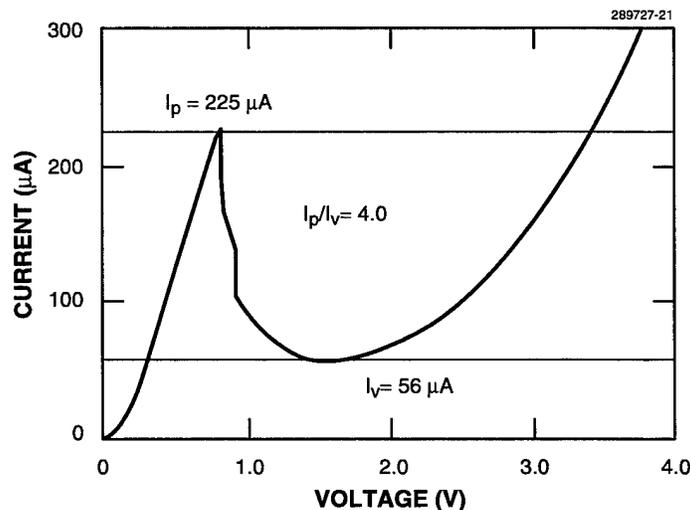


Figure 6-1. Typical resonant-tunneling diode (RTD) current-voltage (I-V) curve.

The conventional RTD fabrication process is based on mesa isolation, resulting in a column of material with an ohmic contact on the top and an embedded RTD layer of limited area. Ohmic metal deposited in the etched region provides contact to the lower side of the vertical RTD. As the two terminals are at different heights, circuit connections require a planarization technique, which adds process steps and can be a source of reduced circuit yield. More recently, a combination of wet etch (on three sides of the RTD) and proton-implant isolation (on the remaining side) has been used to ease the problem of making circuit connection to the small top-side ohmic contact. A significant problem in mesa-isolation RTDs is the uncertainty in device area resulting from variability in the wet-etch process. This leads to significant nonuniformity of device I-V characteristics across the wafer.

We have developed a new self-aligned planar process, based on ion implantation, to overcome the difficulties of wet-etch RTD fabrication. The device geometry is shown in Figure 6-2. The RTD layers are grown, as before, on an SI substrate. Two ion implants, both of which convert the semiconductor material to SI, are used: a shallow boron implant to define the individual RTDs and a deep proton implant to provide isolation between devices. By careful design of both the energy and dose, the boron implant converts the material from the surface down to a level just below the RTD layers, leaving a conducting n^+ layer above the SI substrate for lateral conduction. The process is self-aligned in that the patterned ohmic-contact metal acts as the mask for the boron implant, and its shadow defines the RTD area.

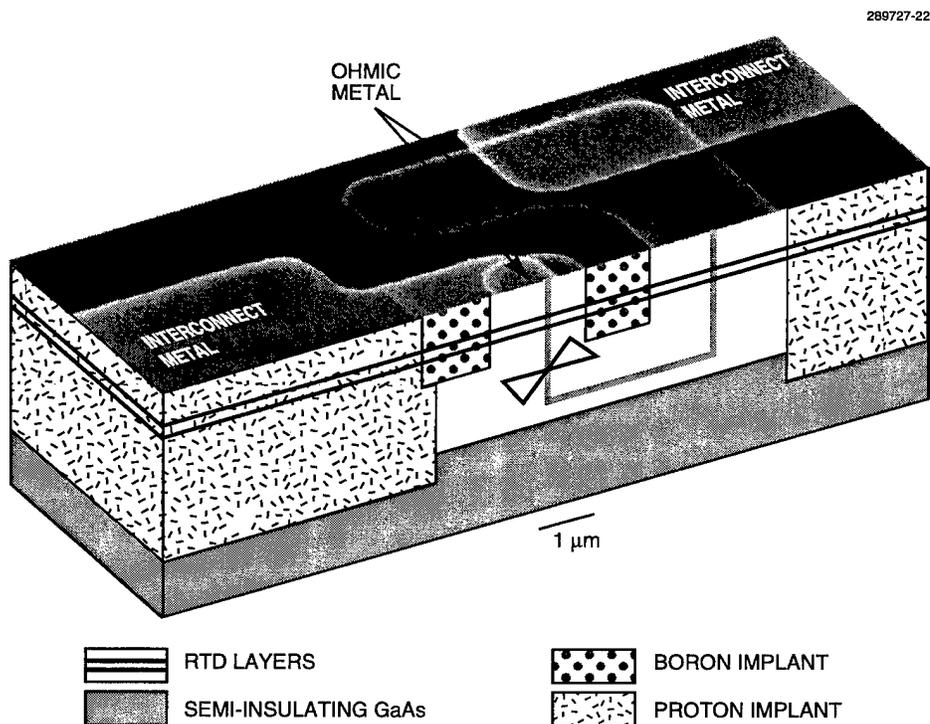


Figure 6-2. Planar self-aligned implant-defined RTD process, illustrated by surface scanning electron micrograph with schematic cutaway of structure.

To create an RTD with planar contacts, two regions of ohmic-contact metal are patterned on the substrate surface in close proximity. Both block the boron implant, preserving the conducting material below. The smaller metal region defines the RTD; the larger metal region defines a contact to the buried n^+ layer. Technically, the larger metal region also defines an RTD; however, because its area is many times larger, it remains biased in the nominally ohmic region below its peak current for all voltages normally encountered in its intended application. A subsequent proton implant surrounds pairs of RTDs and contacts with SI material for device-to-device isolation.

A set of test wafers was fabricated to evaluate the new process, test various device geometries, and derive design rules. The design consisted of 6×10 -mm chips repeated across a 3-in. wafer. While the metal defining all of the RTDs was nominally square, two types of contacts were investigated: square and U-shaped (half of a U-shaped contact is shown in Figure 6-2). Each chip included various sizes of RTDs and contacts, as well as variation in spacing between them. They contained groups of 60 identical RTDs with both square and U-shaped contacts to study uniformity. Chips also included many other test devices: RTDs with Schottky contacts, saturated resistors (gateless FETs), interconnect test structures, and several process evaluation structures.

The test chips were fabricated on RTD wafers grown by gas-source molecular beam epitaxy (MBE) on 3-in. SI GaAs substrates. The RTD layers consisted of an In(14%)Ga(86%)As well between two AlAs barrier layers. Above and below the barriers was 250 nm of 1×10^{17} GaAs. Above the upper layer, a graded InGaAs layer was grown to allow a nonalloyed, nongold ohmic contact, as required to permit the fabrication of these circuits in our Microelectronics Laboratory. (In areas where a Schottky contact is required, that ohmic layer was etched away prior to Al deposition; that is, both ohmic contacts and Schottky contacts are formed during a single metal deposition.) The RTD peak-current density of these wafers was found to be 6–7 kA/cm² with a current peak-to-valley ratio of 4.

An etched Ti-W-Al process, common to silicon processing, was used for the RTD-mask/ohmic-contact layer. After the implants, a second aluminum layer was deposited and patterned to provide probe pads and connections to the various test devices. An important feature of the test chips is the layout of probe pads to permit automatic probing of the thousands of devices on the wafer. This allowed for computer-controlled acquisition and evaluation of a large amount of data. As a consequence, the device density is low, with an average separation of 175 μ m.

The uniformity of RTD peak currents is of primary importance for the proper functioning of most RTD binary circuits. Locally, the RTDs' peak currents must be consistently within a narrow range. Measurements of the I-V relations taken from the groups of 60 identical RTDs are a useful indication of the consistency of this fabrication process. Comparing the average peak currents of these groups from various chips provides a measure of the wafer uniformity of the RTD layers.

Figure 6-3 shows a histogram of the peak currents for one such set of 60 RTDs. The nominal area of the RTDs is $2 \times 2 \mu$ m. The standard deviation is calculated to be 2.3%. This is to be compared to an estimated standard deviation of 6.4% for the previous fabrication technique (using a combination of proton implant and wet etch to define the RTDs).

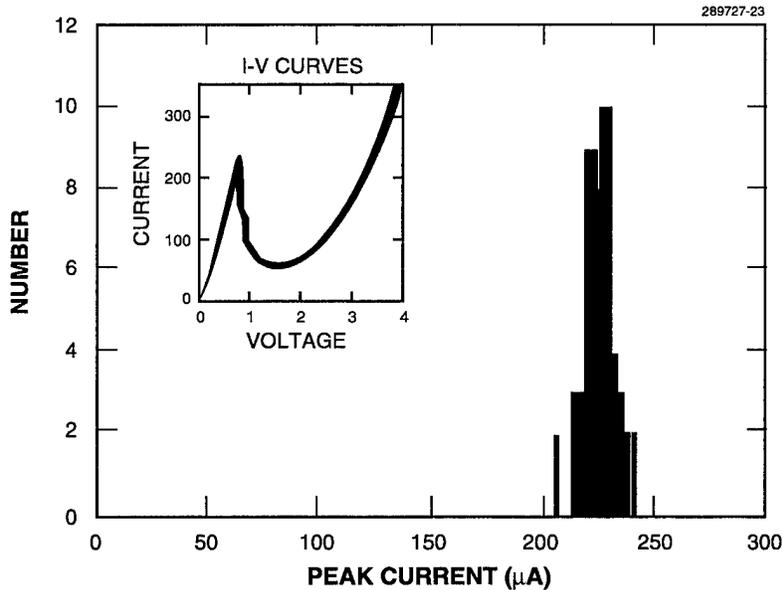


Figure 6-3. Chip level device uniformity illustrated by histogram of peak currents from 60 neighboring (2×2 -mm area) 2×2 - μm RTDs of identical layout. The inset shows an overlay of I-V curves of the same 60 RTDs.

To illustrate the impact of improving the peak-current uniformity, we studied the relation between the range of peak currents that allows for proper operation and the upper limit on the clock frequency for various RTD logic gates. While even perfectly made circuits would have a well-defined clock frequency maximum, variations in the RTDs' peak currents from their ideal values can be accommodated by operating the circuit at a lower clock frequency. Figure 6-4 shows the results of calculations that relate the standard deviation of the RTD fabrication process to the estimated circuit yield for circuits containing 10, 100, and 1000 XORs operating at 40% of their maximum clock frequency. (Calculations have been carried out for all the basic logic gates; the XOR gate is the most demanding in terms of margins and has the lowest maximum clock frequency of these gates.) For a standard deviation of 6.4%, a circuit containing only 10 XORs would have an estimated yield of only a couple of percent, while for a 2.3% standard deviation, the estimated yield of that circuit goes up to 90%, and a circuit containing 100 XORs could have a yield of almost 50%. This demonstrates that the recently developed RTD fabrication process is sufficient for constructing modest-size signal processing circuits. As shown, the maximum allowable circuit complexity increases rapidly as device uniformity is improved below 2% standard deviation. We expect further improvements in uniformity as this process matures.

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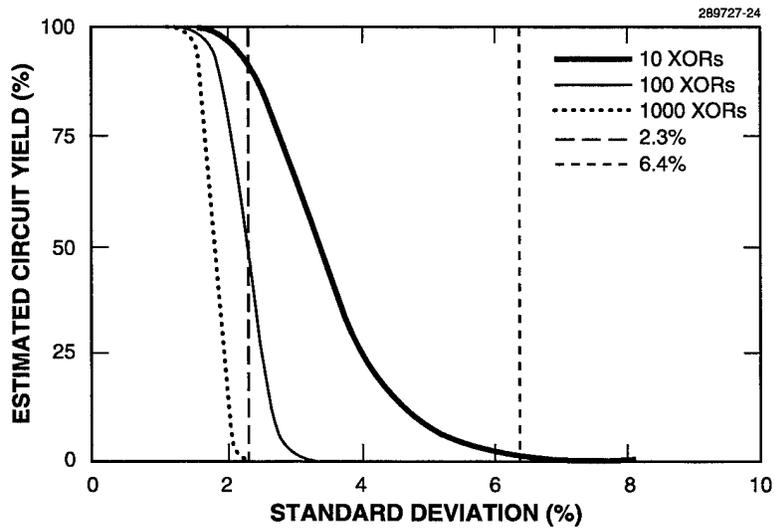


Figure 6-4. Estimated circuit yield as a function of standard deviation in RTD peak currents for various levels of circuit complexity based on calculations for an XOR gate.

7. ADVANCED SILICON TECHNOLOGY

7.1 1.3-GHz SILICON-ON-INSULATOR CMOS TEST CHIP FOR A SUPERCONDUCTIVE COMPRESSIVE RECEIVER

The Analog Device Technology group at Lincoln Laboratory has been developing a compressive receiver system based on high-critical-temperature superconducting delay lines used as chirp filters [1]. Incoming signals are mixed with a swept local oscillator and then passed through the superconducting chirp filter. Continuous frequencies in the input signal emerge as compressed pulses, where the delay of the pulse relative to the start of the sweep is a linear function of the incoming signal's frequency. The chirp filter output is envelope detected, log amplified, and then sampled at 3.2 G-samples per second. The utility of such a receiver depends on the availability of fast, low-power digital electronics for processing the samples of the compressed pulses.

The Lincoln Laboratory SOI CMOS process with 0.25- μm gate lengths seemed to meet the requirements, so a test chip was made, as part of a multiproject wafer run, to demonstrate the suitability of this process for the compressive receiver. The test chip was not a prototype of the pulse processor, but it contained circuits of the type that would be needed in pulse processing: shift registers, binary comparators, and FIFO storage. There was enough complexity (5000 transistors) to give some confidence about process yield. The design also featured onboard decoupling capacitors and self-testing circuits, which together allowed the test chip to be exercised at clock rates above 1 GHz on a probe tester capable of only 20 MHz.

A schematic of the test chip is shown in Figure 7-1. The test chip accepts 8-bit data into its 16-stage shift register. Then it shifts the data into a 16-word FIFO. As the data is shifted past the comparators (labeled C), two adjacent words are compared and the 1-bit result of the comparison is also stored in the FIFO. Finally, the FIFO is read out to the output pins. There are externally controllable options to store only words for which the comparison succeeds or to output the last stage of the shift register rather than the FIFO output bus. The FIFO is always read out with the external unload signal, but the clocking of the shift register and the loading of the FIFO can be done with either an external clock or the fast internal clock. The internal clock is derived from an on-chip ring oscillator, selectable to have 3, 5, 9, or 15 stages. In addition the user can select $\times 1$, $\times 2$, or $\times 4$ frequency division. These selections were designed to give a clock range of 0.20–2.36 GHz with a 2.0-V power supply. The clock frequency is divided by 1024 to drive an output pin for monitoring the actual clock frequency.

The chip is tested at high speeds by first loading its shift register with the test data at low speed, using the external clock. Then the FIFO is reset, producing a single "1" in the leftmost position of both the "insel" and "outsel" registers. Next the fast internal clock is selected. Each clock pulse shifts the 8-bit values along the shift register, past the comparator, and to the FIFO input. On each clock for which loading is enabled, the single "1" in the "insel" register causes the loading of the FIFO input data into the currently selected position and then is shifted right to select the next position. When the "1" is shifted off the right end of the "insel" register, no further writing occurs in the FIFO, even though the clock is still running. Finally the FIFO is read sequentially to the output pins by the slow, external "unload" signal. In this way fast internal operation of the test chip is achieved without any fast clocks or data streams passing through the package pins.

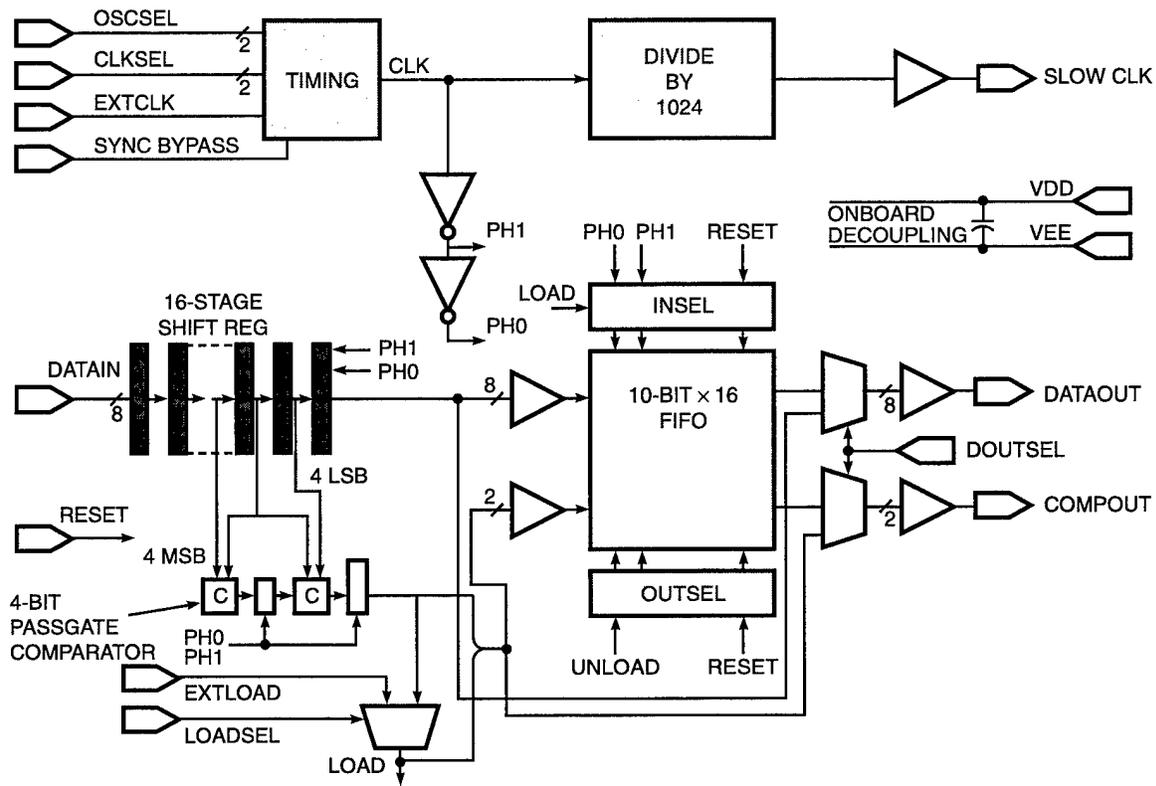


Figure 7-1. Silicon-on-insulator CMOS test chip for compressive receiver.

However, when the fast internal clock is being used, there is still one possibility of a fast “signal” at the package pins, namely, the current transients drawn from the power supply. The decoupling capacitors, Figure 7-2, were designed to supply any surges in current from on the chip, bypassing any series impedance of the power pins. Four capacitors are distributed around the chip, with a total capacitance of 480 pF. This large a capacitance could not be achieved with metal-to-metal or metal-to-poly capacitance, because the dielectric is too thick, on the order of hundreds of nanometers. Instead the gate oxide (8 nm thick) was used as a dielectric. The plates of the capacitor are the lower surface of polysilicon (positive) and an accumulation layer at the top of n -doped silicon (negative). Because the sheet resistance of the accumulation layer is so high, the necessary low series impedance of the capacitor was achieved by a two-dimensional grid of metal 1 contacts on 3.25- μm centers to n^+ -doped silicon abutting the accumulation layer regions. In each five-by-five portion of this grid of contacts, two are missing, replaced by a single contact from the polysilicon plate of the capacitor to metal 2. This is sufficient because the sheet resistance of the silicided polysilicon is much lower than that of the accumulation layer.

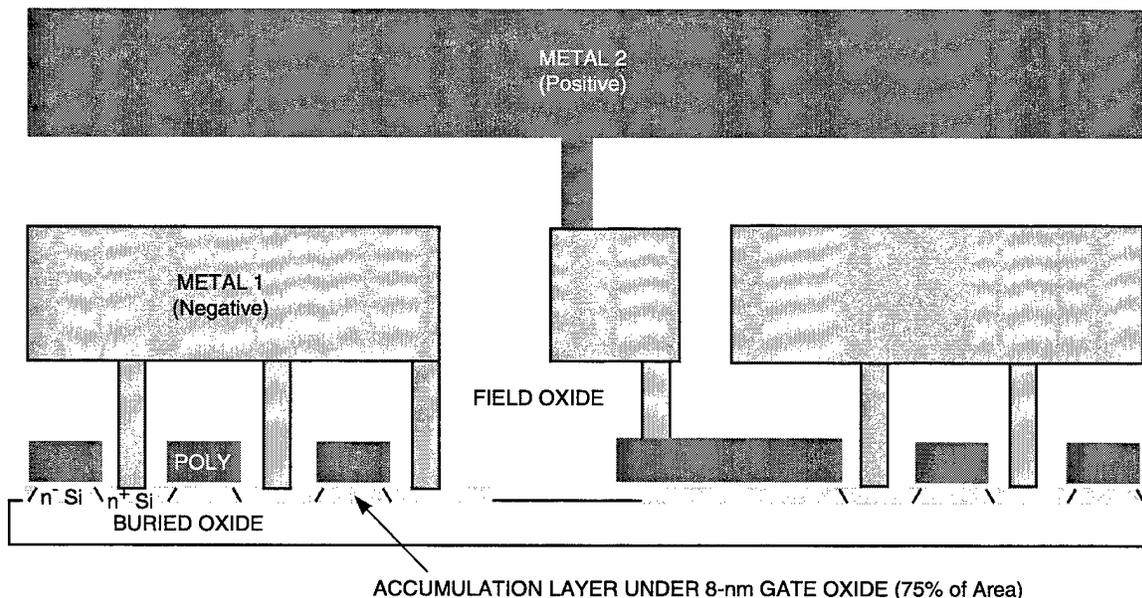


Figure 7-2. Cross section of decoupling capacitor; four capacitors are distributed around the chip.

To be effective as decouplers the capacitors must have an area of gate oxide greatly exceeding the combined gate area of all the logic transistors that could be switching at any one time. Therefore the capacitors are the places most likely to have a short in the gate oxide. Any such short would be directly across the power rails. Thus, the connection of one end of the capacitor to its power rail was designed to be cuttable by laser. No such cutting was needed during the testing of the chips.

The chip was tested on a wafer prober in the procedure described above: load data slowly; shift, compare, and load FIFO fast; unload FIFO slowly. At each choice of power supply voltage, increasingly higher operating frequencies were selected from the discrete set of frequencies selectable for the internal clock. The lower curve in Figure 7-3 plots the highest frequency at which the circuit performed correctly the comparison and the transfer from the shift register to the FIFO. The upper curve plots the highest frequency for which the transfer succeeded, but the comparison had some failures. At 2.6 V, full operation occurred at 1.34 GHz. At the design voltage, 2.0 V, 1.02-GHz operation was achieved, in good agreement with HSPICE simulations.

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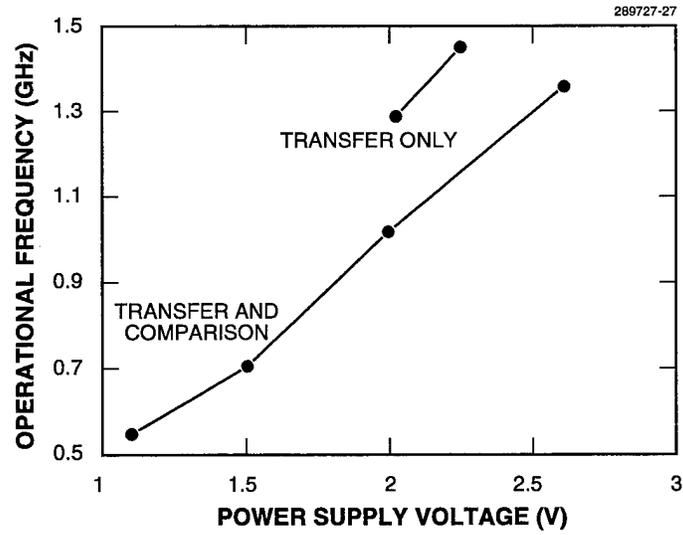


Figure 7-3. Compressive receiver test circuit results.

REFERENCE

1. W. G. Lyons, D. R. Arsenault, A. C. Anderson, T. C. L. G. Sollner, P. G. Murphy, M. M. Seaver, R. R. Boisvert, R. L. Slattery, and R. W. Ralston, *IEEE Trans. Microwave Theory Tech.* **44**, 1258 (1996).

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